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(54) Programmable gate array with improved interconnect structure, input/output structure and configurable logic block.

(57) A programmable gate array with an improved interconnect structure facilitates multi-source networks, communication of signals long distances across the array, and creation of networks in a symmetrical interconnect structure. The interconnect includes direct connections for each configurable logic block in the array to eight neighbors, including adjacent configurable logic blocks and next adjacent configurable logic blocks. Also, the interconnect includes uncommitted long lines which are driven by outputs of configurable logic blocks but not committed through the interconnect to inputs of any specific logic block. Rather, the uncommitted long lines are committed to connections to other segments of the interconnect. The interconnect structure also includes staggered switching matrices at the intersections of the horizontal and vertical buses in the interconnect. Repowering buffers that are configurable in both directions are associated with bidirectional lines in the interconnect, and include a bypass path. The interconnect provides for communication of control signals from off the chip, from any configurable logic block in the array, and from the input/output structures in the array to any or all other configurable logic blocks and input/output blocks in the array.

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In the prior art configurable logic blocks, typically four input signals are used for the logic function. In order to obtain a five variable gating function, the configurable logic blocks used a sharing of inputs scheme. This sharing of inputs greatly limits the logic flexibility for these five variable functions in the prior art.

Prior art configurable logic blocks also suffered speed penalties because of the relatively complex structure required for the blocks to achieve user flexibility. For a block which is being used for a simple function, the logic would be propagated at a relatively slow rate because of the complex structures required.

It is desirable to provide a programmable gate array which provides for greater flexibility and logic power than provided by prior art devices.

Summary of the Invention

The present invention provides an architecture for a configurable logic array with an interconnect structure which improves flexibility in creating networks to allow for greater utilization of the configurable logic blocks and input/output blocks on the device.

Accordingly, we will describe is an improved configurable logic array comprising a configuration memory storing program data specifying a user defined data processing function. In addition, a plurality of configurable logic blocks are arranged in an array consisting of C columns and R rows. Each configurable logic block is coupled to the configuration memory and has a plurality of inputs and outputs for generating output signals at the respective outputs in response to the input signals at the respective inputs and in response to program data in the configuration store. A plurality of configurable input/output blocks is included, each coupled to an input/output pad and to the configuration store, and having at least one input and at least one output. The configurable input/output blocks provide configurable interfaces between the respective pads and the respective inputs and outputs in response to the program data. A configurable interconnect is coupled to the configurable logic blocks, configurable input/output blocks and to the configuration store, for connecting the inputs and outputs of configurable logic blocks and configurable input/output blocks into logical networks in response to the program data in the configuration store.

According to one aspect of the invention, the configurable interconnect is symmetrically disposed relative to the inputs and outputs of the configurable logic blocks. Thus, inputs of the CLBs can be derived from four sides and outputs can be driven to four sides of the respective CLB into a symmetrical interconnect structure.

The interconnect includes a plurality of horizontal buses along the rows of CLBs and a plurality of vertical buses along the columns of CLBs. The intersections of the horizontal and vertical buses are configurable to route networks across the device.

Another aspect of the interconnect includes a plurality of switching matrices at the intersections of horizontal and vertical buses, each having a set of horizontal connections and a set of vertical connections, for interconnecting respective ones of the horizontal or vertical connections in response to program data in the configuration store. A plurality of horizontal conductive segments in the horizontal bus are connected between the horizontal connections of the switching matrices. A plurality of programmable interconnect points coupled to respective inputs and outputs of the configurable logic blocks and input/output blocks provide connectability to respective horizontal segments in response to program data. Likewise, a plurality of vertical conductive segments in the vertical bus are connected between the vertical connections of the adjacent switching matrices. Programmable interconnect points interconnect the respective inputs and outputs of configurable logic blocks and input output blocks with respective vertical segments in response to the program data. The vertical and horizontal segments, according to one aspect of the invention, are characterized by extending from a switching matrix in a vertical or horizontal bus "i" to switch matrix in bus "$i+2^n$", so that each segment spans two columns or rows of logic blocks.

The buses in the interconnect are further characterized by a plurality of horizontal and vertical long conductive lines which extend across the entire chip. Each long line is connected to a plurality of programmable interconnect points for interconnecting the respective inputs or outputs of configurable logic cells with the respective long line in response to program data in the configuration memory. The long lines are characterized by having programmable interconnect points coupling an output of a configurable logic block which is supplied by a tristate buffer to the respective long lines.

In another aspect, the buses in the interconnect structure are characterized by uncommitted horizontal and vertical long lines. Each uncommitted long line is connected to a first plurality of programmable interconnect points for interconnecting the respective outputs of configurable logic blocks or input/output blocks with the respective long line in response to program data, and a second plurality of programmable

fourth level of multiplexing which is controlled by one of the subset of K signals, providing output which is a full lookup function of the 64 bit array in response to six inputs.

The combinational logic further includes a special 16 bit array in the program data which is coupled to a sixteen to one multiplexer. Control inputs to the sixteen to one multiplexer are the pass through outputs of the four cross-multiplexers referred to above. Each of these inputs is a function of four independent variables. The output of the sixteen to one multiplexer provides a special output, which provides a limited lookup function of the 16 independent variables. The special output is combined with the output of the fourth level multiplexer in a fifth level multiplexer, which is controlled in response to an input signal of the subset of K signals, or by the program data.

According to another aspect, the configurable logic block is characterized by a preload capability. During programming of the configurable logic array, each of the storage elements in the output macro cells of the configurable logic blocks is enabled to receive data as if it were a location in the configuration memory.

The configurable input/output architecture, according to the present invention, is characterized by a number of improvements over the prior art. In particular, the architecture provides for groups of input/output blocks associated with each row and column of configurable logic blocks in the array. Each of the groups is further characterized by having a plurality of complex input/output blocks, which provide flexible structures for implementing interfaces between the configurable logic array and outside devices, and at least one simple input/output block which provides a fast path from outside the device to the configurable logic array if required by a particular application.

Further, both the simple and complex input/output blocks are characterized by having at least one tristatable output buf fer for driving signals onto the configurable interconnect structure, and a second buffer for driving direct connections to configurable logic blocks in the device.

The complex input/output blocks include an input storage element and an output storage element. A direct connection is provided from the input storage element of one complex input/output cell to a next adjacent complex input/output around the perimeter of the device. The output storage elements of the complex input/output cells are similarly connected. Thus, the storage elements in the complex input/output blocks can be linked into a configurable data path where they can be operated as a shift register or other similar circuit.

The storage elements in the complex input/output blocks are further configured to provide for synchronization functions, local readback functions, and buried register functions.

The input/output blocks, according to the present invention, are further characterized by control signal generation from the long lines in the programmable interconnect structure. This allows utilization of networks in the configurable logic array to control the operation and configuration of the configurable input/output blocks in a dynamic fashion. Also, the long lines are configured to propagate signals completely around the perimeter of the array, so that a common signal can be used to control all of the input/output blocks.

The configurable logic array provided, according to the present invention, greatly improves the flexibility and performance of programmable gate arrays over those available in the prior art. This is accomplished in part by an interconnect structure which supports networks with long reach across the device, multi-source networks, and symmetrical connections to the configurable logic blocks.

Further, a unique configurable logic block architecture supports efficient utilization of the resources in the array, wide gating functions, narrow gating functions without speed penalty and implementation of symmetrical networks in the array.

Finally, a unique input/output architecture supports efficient utilization of the resources in the input/output structures, allows for both fast signal propagation through the simple input/output blocks and high function signal propagation through the complex input/output blocks into the array, and has improved flexibility in the source of control signals for the input output structure.

Further aspects and advantages of the present invention will be found upon review of the drawings, the detailed description and the claims which follow.

Brief Description of the Figures

Fig. 1 is schematic diagram illustrating the slayout of the programmable gate array according to the present invention.

Fig. 2 is a schematic diagram of the configuration memory in the programmable gate array according to the present invention.

Fig. 35 is a schematic diagram of the input multiplexer structure for signals VC1-VC4 which are used in the first level multiplexing in the combinational logic section of the configurable logic block.

Fig. 36 is a schematic diagram of the input multiplexing structure for signals VD1-VD4 which are used in the second level multiplexing in the combinational logic section of the configurable logic block.

Fig. 37 is a diagram of the input multiplexing structure for VE1 and VE2 used in the third level multiplexing of the combinational logic.

Fig. 38 is a diagram of the input multiplexing structure for the fourth level multiplexing signal VF in the combinational logic.

Fig. 39 is a schematic diagram of the input multiplexing structure for the control signal VG used in providing the special output.

Figs. 40A-40H show respectively the input multiplexing for the general purpose control lines CT1-CT8.

Fig. 41 is a schematic diagram of the circuit generating output enable control signals OE1-OE4 in the configurable logic block.

Fig. 42 is a diagram illustrating selection of the clock signal in the configurable logic block.

Fig. 43 is the schematic diagram illustrating generation of the clock enable signal in the configurable logic block.

Fig. 44 is a schematic diagram illustrating selection of the reset signal in the configurable logic block.

Fig. 45 is a schematic diagram of a simple input output cell according to the present invention.

Fig. 46 is a schematic diagram of a complex input output cell according to the present invention.

Fig. 47 illustrates the inputs and outputs of the complex input/output block.

Fig. 48 illustrates the inputs and outputs of the simple input-output block.

Fig. 49 schematically illustrates the connection of the complex input/output blocks in a shift register configuration.

Fig. 50 illustrates the direct connections from outputs of next adjacent configurable logic blocks to the inputs of a given logic block.

Fig. 51 illustrates direct connections from adjacent configurable logic blocks to the inputs of the center configurable logic block.

Fig. 52 illustrates direct connections from the output of the center configurable logic block to adjacent and next adjacent configurable logic blocks.

Fig. 53 illustrates direct connection of the outputs X1-X4 on peripheral configurable logic blocks.

Fig. 54 illustrates direct connection to the inputs of a peripheral configurable logic block.

Fig. 55 illustrates direct connections to the inputs F1-F4 on a peripheral configurable logic block.

Fig. 56 illustrates the programmable connections between the interconnect structure and the configurable logic blocks.

Fig. 57 illustrates the fixed connections between the interconnect structure and the configurable logic blocks.

Fig. 58 illustrates the programmable connection of the configurable logic blocks in the array to uncommitted long lines.

Fig. 59 illustrates the programmable connections to the outer long lines from the CLBs.

Fig. 60 illustrates the reach between input-output blocks and configurable logic blocks on long lines.

Fig. 61 illustrates the programmable connections between the input/output blocks on the top side of the configurable array and horizontal bus 1.

Fig. 62 illustrates the programmable connections between horizontal bus 9 and the input/output blocks on the bottom side of the configurable array.

Fig. 63 illustrates the programmable interconnects between the vertical bus 1 and the input/output blocks on the left side of the array.

Fig. 64 illustrates the programmable interconnects between vertical bus 9 and the input/output blocks on the right side of the array.

Fig. 65 illustrates the connection of the clock and reset signals to the complex logic blocks, as well as the programmable connections of the inputs and the outputs of the input/output blocks on the top side of the array to the vertical buses.

Fig. 66 illustrates the connection of the clock and reset signals to the input/output blocks on the bottom side of the array, and connection of these bottom side input/output blocks ta the vertical buses.

Fig. 67 illustrates the connection of the clock and reset signals to the input/output blocks on the left side, and connection of these left side input output blocks to horizontal buses.

Fig. 68 illustrates the connection of the clock and the reset signals to the input/output blocks on the right side of the array, and connection of these right side input/output blocks to the horizontal buses.

Fig. 69 illustrates the connection of the control signal inputs on the input/output blocks on the top and left

form networks carrying logic signals among the blocks.

The logic functions performed by the CLBs are determined by programmed lookup tables in the configuration memory. Functional options are performed by program controlled multiplexers. Interconnecting networks between blocks are composed of metal segments joined by programmable interconnect points (PIPs).

The logic functions, functional options, and interconnect networks are activated by a program data which is loaded into an internal distributed array of configuration memory cells. The configuration bit stream is loaded in to the device at power up and can be reloaded on command.

Fig. 2 is a schematic diagram of the programmable gate array as seen by the program data. The programmable gate array includes a plurality of distributed memory cells referred to as the configuration memory 200. Program data on line 201 is loaded into shift register 202 in response to a clock signal on line 203. The detect logic 204 determines when the shift register is full by reading a preamble from data on 201. When the shift register is full, the detect logic 204 signals across line 205 a frame pointer logic 206 which generates frame pointer signals across lines 207. Control logic 208 is responsive to the mode inputs to the device on line 209 to control the detect logic 204 across line 210 and the frame pointer during loading of the configuration memory 200.

The configuration memory 200 is organized into a splurality of frames F1-FN. As program data is loaded into the shift register, the frame pointer F1 is activated to load the first frame in the configuration memory. When the shift register is loaded with the second frame of data, the frame pointer for F2 is activated, loading the second frame F2, and so on until the entire configuration memory is loaded. Control logic 208 generates a program done signal on line 210.

The static memory cell used in the configuration memory is shown in Fig. 3. It has been specially designed for high reliability and noise immunity. A basic cell 300 consists of a data input line 301 coupled to pass transistor 302. The gate of the pass transistor 302 is coupled to a read or write control signal on line 303. The output of the pass transistor 302 is coupled to line 304. Line 304 is coupled to the input of inverter 305 and to the output of inverter 306. The output of inverter 305 is coupled to line 307 which is coupled back to the input of inverter 306. Lines 304 and 307 provide Q and $\overline{Q}$ outputs for configuration control. Thus, the basic cell 300 consists of two CMOS inverters and a pass transistor. The pass transistor is used for writing and reading cell data. The cell is only written during configuration and only read during read-back in the programming mode. During normal operation, the pass transistor is off and does not affect the stability of the cell. The memory cell outputs Q and $\overline{Q}$ use full ground and V_{CC} levels and provide continuous direct control.

The configuration store can also be implemented with other types of volatile or non-volatile storage cells. For instance, non-volatile memory, like EPROM, E^2PROM, programmable resistive links, or Ferro RAM, could be used.

The device memory is configured as mentioned above by downloading a bit stream from a host system or an external memory, such as an EPROM. The configuration processes are the same as those used in prior art programmable gate array, with one exception which is discussed below with reference to the configurable logic blocks.

II. The Configurable Interconnect Structure

Horizontal and vertical buses of the interconnect structure and the interconnection of the horizontal and vertical buses are described with reference to Figs. 4-24.

Fig. 4 illustrates the notation used for the vertical buses. Each vertical bus has 25 lines. Lines 1-4 and 15-17 are long lines which run across the entire array. Lines 5-14 consist of bidirectional general interconnect segments which are coupled through switching matrices and segment boxes as described below. Lines 18-25 are uncommitted long lines which run the entire length of the array.

Fig. 5 illustrates the notation used for the horizontal buses. Each horizontal bus is a 23 line bus in which lines 1-4 and 15 are long lines, lines 5-14 are bidirectional general interconnect segments, and lines 16-23 are uncommitted long lines. The distinctions between the long lines, the bidirectional general interconnect segments, and the uncommitted long lines are set out in detail below.

In order to construct networks through a device, the horizontal and vertical buses require means of interconnection. This occurs at the intersections of the horizontal buses and the vertical buses. The interconnections between the lines at the intersection are made through programmable interconnect points, switch matrices, and segment boxes.

Fig. 6 illustrates the placement of the switch matrices in the interconnectstructure.

vertical lines 1-4. The bidirectional general interconnect segments 5-9 are connectable to the vertical segments 5-9 and to the even numbered uncommitted long lines 18, 20, 22, and 24 as shown. The horizontal bidirectional general interconnect segments 10-14 are connected to the segment box in both the horizontal and vertical directions. The even numbered uncommitted long lines 16, 18, 20, and 22 on the horizontal bus are connectable to vertical bidirectional general interconnect segments 6-9 as shown.

The corner intersections are shown in Figs. 11-14. Fig. 11 illustrates the intersection of horizontal bus 1 with vertical bus 1. As shown, the lines 1-14 in the horizontal bus are connectable respectively to lines 1-14 in the vertical bus. The even numbered uncommitted long lines 18, 20, 22, and 24 on the vertical bus are connectable to horizontal bidirectional general interconnect segments 6-9. The even numbered uncommitted long lines 16, 18, 20, and 22 on the horizontal bus are connectable to the vertical lines 6-9.

Fig. 12 illustrates the intersection of horizontal bus 1 with vertical bus 9. In this instance, the horizontal line 1 is connectable to vertical lines 1 and 4. Horizontal line 2 is connectable to vertical lines 2 and 3. Horizontal lines 3-14 are connectable respectively to vertical lines 3-14. The even numbered uncommitted long lines 18, 20, 22, and 24 on the vertical bus are connectable to horizontal lines 6-9. The even numbered uncommitted long lines 16, 18, 20, and 22 on the horizontal bus are connectable to the vertical lines 6-9.

Fig. 13 illustrates the intersection of horizontal bus 9 with vertical bus 1. The horizontal lines 1-14 are connectable to the vertical lines 1-14, respectively. Also, horizontal line 3 is connectable to vertical line 2 and horizontal line 4 is connectable to vertical line 1. The horizontal lines 6-9 are also connectable to the even numbered uncommitted long lines 18, 20, 22 and 24 on the vertical bus. The even numbered uncommitted long lines 16, 18, 20 and 22 on the horizontal bus are connectable to vertical lines 6-9.

Fig. 14 illustrates the intersection of horizontal bus 9 with vertical bus 9. Horizontal lines 1-14 are connectable to vertical lines 1-14, respectively. Horizontal lines 6-9 are also connectable to the even numbered uncommitted long lines 18, 20, 22 and 24 on the vertical bus. The even numbered uncommitted long lines 16, 18, 20 and 22 on the horizontal bus are connectable to vertical lines 6-9.

Fig. 14A shows a corner connection that can be used at the intersections of horizontal bus 1 and vertical bus 1, horizontal bus 1 and vertical bus 9, horizontal bus 9 and vertical bus 9, and horizontal bus 9 and vertical bus 1. It has the advantage that it is a single layout that can be used at all four corners while accomplishing the ability to route signals from the long lines 1-4 completely around the perimeter of the chip. As can be seen, horizontal lines 1-14 are connectable to vertical lines 1-14, respectively. Horizontal line 1 is connectable to vertical line 4, horizontal line 2 is connectable to vertical line 3, horizontal line 3 is connectable to vertical line 2, and horizontal line 4 is connectable to vertical line 1. Also, horizontal line 14 is connectable to vertical line 5, horizontal line 13 is connectable to vertical line 6, horizontal line 12 is connectable to vertical line 7, horizontal line 11 is connectable to vertical line 8, horizontal line 10 is connectable to vertical line 9, horizontal line 9 is connectable to vertical line 10, horizontal line 8 is connectable to vertical line 11, horizontal line 7 is connectable to vertical line 12, horizontal line 6 is connectable to vertical 13, and horizontal line 5 is connectable to vertical line 14. Also, horizontal lines 6-9 are connectable to the even numbered, uncommitted long lined 18, 20, 22, and 24 on the vertical bus. Ilhe even numbered long lines 16, 18, 20, 22 on the horizontal bus are connectable to vertical lines 6-9.

Lines 15 on the horizontal and vertical buses and 16 and 17 on the vertical buses are not connectable at any of the intersections described above. Rather, they are designed to be used for local clock/clock enable, global clock, and global reset signals and have special connection structures shown in Figs. 15 and 16. Fig. 15 illustrated the connection of the global clock and global reset signals on vertical lines 16 and 17. The global clock signal is supplied from an input buffer 1500 to line 1501. Line 1501 is directly connected to line 16 in all vertical buses. Similarly, the global reset signal is supplied at global reset buffer 1502. The output of the global reset buffer is supplied on line 1503 to line 17 on all the vertical buses. The lines 16 and 17 of the vertical buses are directly connected to the input/output blocks as schematically illustrated in Fig. 15 and to each of the configurable logic blocks. The direct connections to the configurable logic blocks are shown only to few of the blocks in the upper left hand corner of the array for clarty of the figure.

Fig. 15A shows the connection of lines 16 and 17 of the vertical buses to the configurable logic blocks. The lines 16 and 17 of vertical bus-n are coupled to the global clock GK and global reset GR inputs of configurable logic block in column n, for n = 1-8. In vertical bus 9, lines 16 and 17 are connected only to the input/output blocks as shown.

Fig. 15B shows the configurable path from an input/output pad to an IOB or to the global or alternate buffers. It can be seen that the pad 1510 is connected across line 1511 through buffer 1512 to line 1513. Line 1513 is passed through pass transistor 1514 to an IOB input path 1515 or through pass transistor 1516 to the buffer input circuitry on line 1517. A memory cell 1518 in the configuration store controls which pass transistor (1514 or 1516) is enabled.

Fig. 15C illustrates the input circuitry to the global clock buffer. Input I of IOB 2 and 9 are connected to

the long line, or they can use the alternate buffer as a source.

Fig. 16B illustrates the input structure to the vertical alternate buffer 1603. The input to the vertical alternate buffer 1603 is provided on line 1610 at the output of the configurable multiplexer 1611. Also, the signal on line 1610 is connected for supply as output signals at IOB 1612 and at IOB 1613. Inputs to the multiplexer 1611 include an oscillator signal OSC as generated by the circuitry illustrated in Figs. 16D and 16E. Also, an input signal from IOB 1612 is an alternative input to multiplexer 1611 across line 1614. A vertical clock input signal is supplied on line 1615 as input to multiplexer 1611 from IOB 1616 configured as shown in Fig. 15B.

Long lines 5 and 15 of the vertical bus 9 and long lines 5 and 15 of the horizontal bus 9 are also connected as inputs to multiplexer 1611. The final input to multiplexer 1611 is a direct link from output X2 of the configurable logic block in row 8, column 8, across line 1617.

The vertical alternate buffer 1603 also includes a memory cell 1618 for tristate control.

Fig. 16C illustrates the input structure for the horizontal alternate buffer 1600. The horizontal alternate buffer is tristatable in response to the signal at memory cell 1620. The input to horizontal alternate buffer 1600 is supplied on line 1621 at the output of the configurable multiplexer 1622. Inputs to the configurable multiplexer 1622 include the horizontal clock input signal on line 1623, and input signals on lines 1624 and 1625 from input/output structures 1626 and 1627, respectively. The vertical bus lines 5 and 15 and horizontal bus lines 5 and 15 are connectable as inputs as well to the multiplexer 1622. Finally, a direct link from the configurable logic block in row 8, column 1, output X4 is coupled across line 1628 as an input to multiplexer 1622.

The on chip oscillator which supplies the OSC signal as one input to the multiplexer 1611 driving the vertical alternate buffer 1603 is shown in Fig. 16D. The OSC signal is provided at the output of multiplexer 1630 which is controlled by memory cell 1631. Inputs to multiplexer 1630 include the signal on line 1632 which is supplied at the output of inverting buffer 1633. The input to inverting buffer 1633 is the signal on line 1634 which is supplied at the output of the oscillator amplifier 1635. The input to the oscillator amplifier 1635 is supplied at IOB 1636. IOB 1637 is coupled directly to line 1634. Line 1634 is supplied through inverting buffer 1638 as a clock input on line 1639 to register 1640. Register 1640 is connected as a divide-by-two circuit by coupling line coupled from its Q output through inverting buffer 1642 as the D input to register 1640. The Q output of register 1640 is supplied on line 1643 as a second input to multiplexer 1630.

The external connections for the oscillator are shown in Fig. 16E. Pad 1637 is coupled to line 1650 and pad 1636 is coupled to line 1651. Resistor R1 is sconnected between line 1650 and 1651. Line 1651 is coupled through capacitor C1 to GROUND and through crystal 1652 to line 1653. Line 1653 is coupled through capacitor C2 to GROUND and through resistor R2 to line 1650.

The divide-by-two option in the oscillator circuit is provided to ensure symmetry of the signal. The output of the 2:1 multiplexer 1630 gives this choice, and is set during device configuration. When the oscillator inverter is not used, the paths 1637 and 1636 are configurable as shown in Fig. 15B to behave as standard IOBs.

The oscillator circuit becomes active before configuration is complete to allow it to stabilize.

The structure of the programmable interconnect points (PIPs) is shown in Fig. 17 and an alternative structure is shown in Fig. 18. The structure in Fig. 17 illustrates that for an intersecting conductive segment, such as long lines 1700 and 1701, with long line 1702, a PIP is implemented using a pass transistor. Thus, pass transistor 1703 provides for interconnection between lines 1702 and 1701. Pass transistor 1704 provides for interconnection between lines 1700 and 1702. The memory cell 1705 from the configuration store controls the pass transistor 1703 to provide a bidirectional path between the lines. Likewise, memory cell 1706 controls pass transistor 1704 to provide the bidirectional path. These interconnection points are illustrated throughout this document using the circular symbol 1707 as shown in the figure. Thus, the symbolic representation of the circuit on the left side of Fig. 17 is shown on the right side of Fig. 17.

The PIP implementation of Fig. 17 is advantageous in that it provides for bidirectional connection on the lines which allows for great flexibility. However, this structure is memory intensive. Therefore, an alternative implementation, as shown in Fig. 18, can be used to save memory in a given implementation. The implementation of Fig. 18 illustrates that a PIP can be implemented as a multi-source multiplexer 1800. Multiplexer 1800 can have three sources, source 1, source 2, and source 3, and select a destination line 1801 in response to memory cells 1802 in the configuration store. Using the multiplexer implementation, two memory cells can provide for selection from among three or four sources. The equivalent symbol for the circuit using multiplexer 1800 is shown at 1803. It should be recognized that the multiplexer implementation is a unidirectional interconnect which allows for connection from any one of the source lines to the destination line and not vice versa. Furthermore, only one source line can be activated for a given operation.

segment box has 20 input connections, five on each side, as illustrated in the figure. The input connections 20 and 6 are directly connected, input connections 19 and 7 are connected, inputs 18 and 8 are connected, inputs 17 and 9 are connected, and inputs 16 and 10 are connected. Inputs 1 and 15 are connectable through PIPs to the line connecting inputs 20 and 6. Inputs 2 and 14 are connectable through respective PIPs to the line connecting inputs 9 and 7. Inputs 3 and 13 are connectable through PIPs to the line connecting inputs 18 and 8. Inputs 4 and 12 are connectable through PIPs to the line connecting inputs 17 and 9. Finally,inputs 5 and 11 are connectable through PIPs to the line connecting inputs 16 and 10.

The segment box on the horizontal buses 1 and 9 is shown in Fig. 23. In this implementation, inputs 1 and 15 are connected directly, inputs 2 and 14 are connected directly, inputs 3 and 13 are connected directly, inputs 4 and 12 are connected directly, and inputs 5 and 11 are conected directly. Inputs 20 and 6 are connectable through PIPs to the line connecting inputs 1 and 15, inputs 19 and 7 are connectable through PIPs to the line connecting inputs 2 and 14. Inputs 18 and 8 are connectable through PIPs to the line connecting inputs 3 and 13. Inputs 17 and 9 are connectable through PIPs to the line connecting inputs 4 and 12. Finally, inputs 16 and 10 are connectable through PIPs to the line connecting inputs 5 and 11.

Fig. 24 graphically illustrates in the style of Fig. 21, the possible interconnections for each input to a segment box. These possible interconnections apply equally to the segment boxes on the vertical buses and to the segment boxes on the horizontal buses.

So far, the basic interconnection structure of the programmable gate array has been described without emphasizing the connections to the configurable logic blocks and the input-output blocks. Accordingly, in order to describe those connections, a detailed description of the configurable logic blocks and the input/output blocks follows. Then, the connection of the input/output blocks and configurable logic blocks to the interconnect structure is set out.

III. Configurable Logic Block

A detailed implementation of the configurable logic block is set out with reference to Figs. 25-44. An overview block diagram is set out in Fig. 25.

The configurable logic block 2500 shown in Fig. 25 consists of a combinational function and control generator 2501 which receives inputs from four sides, schematically illustrated by buses 2502-1, 2502-2, 2502-3, and 2502-4. The combinational function and control generator 2501 communicates with four independently configurable output ports 2503-1, 2503-2, 2503-3, and 2503-4. The output ports receive signals and supply feedback signals to and from the combinational function and control generator 2501 across respective buses 2504-1, 2504-2, 2504-3, and 2504-4. Each output port supplies a plurality of output signals, schematically illustrated by the respective output buses 2505-1, 2505-2, 2505-3, and 2505-4.

The block diagram of Fig. 25 illustrates at a high level the symmetry of the configurable logic block 2500. Input signals can be received from all four sides of the block, likewise, output signals can be supplied to any of the four sides of the block. Furthermore, as seen below, input signals from the input bus 2502 can be used to generate output signals across bus 2505-1, 2505-2, 2505-3, or 2505-4. Similar flexibility is provided from all of the other input buses in the configurable logic block.

The inputs and outputs to the configurable logic block are set out in Fig. 26. Also, a notation for the inputs and outputs is provided. It can be seen that input signals along the top side of the bus are labeled A1 through D1, EM1, EN1, FM1, FN1, G1, H1, and K1. The outputs are labelled X1 and Y1. Similarly, the suffix 2 is applied to the right side of the chip, the suffix 3 is applied to the bottom of the chip, and the suffix 4 is applied to the left side of the chip. On the left side of the chip, additional inputs GR and GK for global reset and global clock signals are provided.

As shown in the legend in Fig. 26, the inputs A1 through A4 and B1 through B4 are long line inputs. Inputs C1 through C4 and D1 through D4 are inputs coupled to the bidirectional general interconnect segments for logic signals.

The inputs EM1 through EM4, FM1 through FM4, EN1 through EN4, and FN1 through FN4 are direct connect inputs. The inputs G1 through G4 and H1 through H4 are inputs to the bidirectional general interconnect segments for control signals.

The inputs K1 through K4 are long line inputs from bus line 15 used for clock and clock enable functions.

Outputs are supplied at terminals X1 through X4 and Y1 through Y4. Direct connect structures are connected to X1 through X4. The general interconnect structures are coupled to outputs Y1 through Y4.

The combinational logic block consists of a 64 bit RAM addressed through a multiplexing tree as shown in Fig. 27, 16 additional bits of RAM addressed through a special output multiplexer as shown in Fig. 28,

for the direct connect.

Signal 2903 is also coupled to multiplexer 2905. The second input to multiplexer 2905 is a signal FD1. The output TY1 of multiplexer 2905 is coupled to a tristate output buffer 2906. The output of buffer 2906 is the Y1 signal for connection to the interconnect structure. The tristate buffer 2906 is controlled by the control signal OE1 generated within the configurable logic block as described below.

The register 2901 in the macro cell further has the ability to be preloaded during programming. This functionality is illustrated in Fig. 29A where the signal DQ1 is supplied to a multiplexer 2908. The second input to multiplexer 2908 is program data. The multiplexer 2908 is controlled by the control signal PROGRAM DONE. When PROGRAM DONE is false, the program data is selected through to the D input of the register 2901. Otherwise, the signal DQ1 is supplied. Likewise, the register 2901 is clocked at the output of gate 2909. The gate 2909 provides an OR function with the frame pointer and the output of AND-gate 2910. The inputs to AND-gate 2910 include the clock signal CK generated within the configurable logic block and the inverse of PROGRAM DONE. Thus, during programming stage, the clock signal is disabled and the frame pointer is used to clock register 2901 with program data. After programming is completed, the clock signal is supplied directly through to the register 2901. The same structure is utilized in each of the macro cells, although it is not explicitly shown to clarify the diagrams.

Fig. 30 shows the macro cell supplying the outputs X2 and Y2. The inputs to macro cell 2 in Fig. 30 include FC2, FE2, H, and FD2. FC2, FE2, and H are supplied through multiplexer 3000 to generate the signal DQ2. DQ2 is supplied to register 3001. The output Q2 of register 3001 is supplied as an input to multiplexer 3002. Other inputs to multiplexer 3002 include FC2 and FE2. The output QF2 of multiplexer 3002 is supplied on line 3003 as feedback and directly to output buffer 3004 supplying the signal X2 to the direct connect.

The signal on line 3003 is also supplied to multiplexer 3005. The second input to multiplexer 3005 is the signal FD2. The output TY2 of multiplexer 3005 is supplied as an input to tristate output buffer 3006, which drives the signal Y2. Tristate buffer 3006 is controlled by control signal OE2.

The output macro cell of Fig. 31 drives the signals X3 and Y3. Its inputs include the signals FC3, FE1, D1, H and FD3. The inputs FC3, FE1, and D1 are coupled through multiplexer 3100 to supply the signal DQ3. Signal DQ3 is coupled to register 3101. The output Q3 of register 3101 is supplied as an input to multiplexer 3102. Two other inputs to multiplexer 3102 include FC3 and H. The output QF3 of multiplexer 3102 is supplied on line 3103 as feedback and directly to the buffer 3104 which drives the signal X3. Also, the signal on line 3103 is supplied to multiplexer 3105. The second input to multiplexer 3105 is signal FD3. The output TY3 of multiplexer 3105 is supplied to the tristate buffer 3106 driving the signal Y3. The tristate buffer 3106 is controlled by the signal OE3.

The output macro cell for the driving signals X4 and Y4 is shown in Fig. 32. It is similar to the macro cell of Fig. 31. The input signals include FC4, FE2, D2, H, and FD4. The signals FC4, FE2 and D2 are supplied through multiplexer 3200 to supply the signal DQ4. Signal DQ4 is supplied through register 3101 to generate the output signal Q4. The output signal Q4 is supplied to multiplexer 3102. Other inputs to multiplexer 3102 include FC4 and H. The output of multiplexer 3102 is the signal QF4 on line 3203 which is supplied as feedback and is coupled to buffer 3204 to drive the signal X4. The signal on line 3203 is also supplied to multiplexer 3205. A second input to multiplexer 3205 is the signal FD4. Multiplexer 3205 generates a signal TY4 which is coupled to the tristate buffer 3206. Tristate buffer 3206 is controlled by the signal OE4 and drives the output Y4 of the configurable cell.

A design goal of the macro cells is to provide symmetrical function of each of the macro cells. Accordingly, to provide greater symmetry, the macro cell 1 and macro cell 2 could be changed to allow for the addition of input signals D3 and D4, respectively, at the input multiplexers 2900 and 3000. Further, the ability to provide the signal H in either a registered or combinatorial function could be allowed at each of the macro cells. The same is true for the signals FE1 and FE2. However, to optimize utilization of the die in the preferred embodiment, the macro cells shown in Figs. 29-32 have been adopted. Complete symmetry would be attained by replacing the 3:1 muxes with 4:2 muxes in Figs. 29-32.

Note that the macro cells of Figs. 31 and 32 provide for utilization of the registers 3101 and 3201 even if they are not used for driving the output of the combinational logic. This is provided by allowing the inputs D1 and D2 to be directly coupled to the registers in the output macro cells.

Although not shown in Figs. 29-32, each register includes a clock, clock enable and reset control. Furthermore, each of the multiplexers shown in the figures, unless a dynamic control signal is explicitly shown, is controlled by memory cells in the configuration program. Thus, the configuration of the macro cells is set during programming of the device. Note that each of the macro cells receives signals from the second level of multiplexing, the third level of multiplexing, and the output signal H.

Note also that the macro cell allows the output X1 and the output Y1 to be driven from different sources

Fig. 40F illustrates generation of the signal CT6 by multiplexer 4006 in response to inputs G3 and G4.

Fig. 40G illustrates generation of the signal CT7 by multiplexer 4007 in response to inputs H1 and H2.

Fig. 40H illustrates generation of the signal CT8 by multiplexer 4008 in response to inputs H3 and H4.

Fig. 41 illustrates generation of the output enable signals OE1 through OE4 used in the output macro cells of Figs. 29-32. Each of the signals OE1 through OE4 is independently supplied by respective multiplexers 4100, 4101, 4102 and 4103. The inputs to multiplexers 4100, 4101, 4102 and 4103 include V_{CC} and the common OE control signal on line 4104. The signal on line 4104 is generated at the output of 4:1 multiplexer 4105. 4:1 multiplexer 4105 is coupled to four memory cells in the configuration memory 4106. Multiplexer 4105 is controlled by the signals CT5 and CT6. Thus, each output enable signal can be configured to be statically enabled by selecting this V_{CC} as the output signal. Alternatively, it can be dynamically enabled or disabled in response to the common OE control signal on line 4104. Further independence of programming can be accomplished by providing independent dynamic signals for use as the output enables.

Fig. 42 illustrates generation of the clock signal CK which is used to clock the registers in the output macro cells. This signal is generated at the output of 2:1 multiplexer 4200. The inputs to the 2:1 multiplexer 4200 include a true and complement version of the signal supplied on line 4201 at the output of 6:1 multiplexer 4202.

Multiplexer 4202 receives as inputs the signals K1 through R4 from bus line 15 on four sides of the macro cell, the input GK from the global clock lines, and the control signal CT7. The multiplexers in Fig. 42 are configured by memory cells in the configuration memory.

Fig. 43 illustrates generation of the clock enable signal which is coupled to the registers in the output macro cells. The clock enable signal is generated at the output of multiplexer 4300. The input to multiplexer 4300 includes a signal on line 4301 which is supplied at the output of the 3:1 multiplexer 4302. The second input to multiplexer 4300 is the V_{CC} signal. Thus, the clock enable signal can be permanently enabled by connection to V_{CC}. The inputs to multiplexer 4302 include the K1 signal, K2 signal and the control signal CT7.

Fig. 44 illustrates generation of the reset signal RST which is supplied to the registers in the output macro cells in the configurable logic block. The reset signal is generated at the output of OR-gate 4400. The inputs to OR-gate 4400 include the signal on line 4401 which is generated at the output of multiplexer 4402. The other input to OR-gate 4400 is the global reset signal GR. The two inputs to multiplexer 4402 include CT8 and GROUND. Thus, the reset signal CT8 can be permanently inhibited by connection to GROUND. Global reset is always allowed.

Thus, the configurable logic block described above provides for symmetrical interfaces on all four sides of the block to the interconnect structure. Furthermore, it allows for wide gating and narrow gating functions without suffering a speed penalty for the narrow gated functions. Furthermore, the wide gating functions do not require sharing of input signals which complicates logic design using the configurable logic block.

IV. The Input/Output Block

The configurable input/output blocks in the programmable gate array of the present invention consist of a simple block as shown in Fig. 45 and a complex block as shown in Fig. 46. Each input/output block (IOB) is coupled to memory cells in the configuration memory, the states of which control the configuration of the IOB. In general, an IOB allows data to pass in two directions: (i) from an input/output pad to the programmable general connect and specific CLBs; (ii) from the programmable general connect and specific CLBs to a pad.

The configuration of an IOB sets the type of conditioning the signal receives on passing through the IOB. The pad may or may not be bonded to a physical package pin.

There are two types of IOBs in the device. A simple IOB as shown in Fig. 45 with combinatorial input and output only. Also, a complex IOB as shown in Fig. 46 provides an input register/latch and an output register in addition to combinatorial features. The complex IOB also has internal links for giving the user input register read-back at the package pin, and direct links to adjacent complex IOBs that allow data to be transferred to the registers of an adjacent IOB.

Note that the silicon die can be put into packages having more than, less than, or the same number of package pins as there are IOB pads on the die. If there are fewer package pins than IOB pads, then some IOBs may not be linked to a device package pins and so become buried IOBs for internal device use.

As suits the needs of a particular user, the number of simple IOBs and complex IOBs on a given implementation may vary due to die size and speed constraints. Further, the PGA could include all simple

The output Q1 of the register/latch 4615 is supplied on line 4621 as an input to multiplexer 4622, as an input to multiplexer 4623, and as the Q1 output ssignal on line 4606, and input to the multiplexer 4640.

A second input to multiplexer 4622 is the PI signal on line 4610. A third input to multiplexer 4622 is the output of the output register on line 4624 as described below. The output of multiplexer 4622 is supplied to line 4625. Line 4625 is coupled as input to buffer 4626 which drives line 4602 to the direct connect, and as an input to buffer 4627 which is a tristate buffer driving connections to the long lines on line 4601. Buffer 4627 is controlled by the tristate input signal on line 4628. The signal on line 4628 is supplied at the output of the 4:1 multiplexer 4629. Inputs to the 4:1 multiplexer 4629 include the V_{CC} signal, IEN in its true and complement form, and GROUND.

The output path through the complex IOB is connected to receive the signal O on line 4630 at the output of multiplexer 4603. The signal O on line 4630 is supplied as the second input to multiplexer 4623. The output of multiplexer 4623 is supplied as input to multiplexer 4631. The second input to multiplexer 4631 is supplied at the output of multiplexer 4632. The inputs to multiplexer 4632 are the QP1 and QP2 signals. The output of multiplexer 4631 is the D2 signal on line 4633. The D2 signal is coupled as data input to the output register 4634.

The output register 4634 is coupled to the global sreset signal GR on line 4635. It is clocked by the signal K2 on line 4636 which is generated at the output of multiplexer 4637. Inputs to multiplexer 4637 include the global clock GK, the K signal, and the CEN signal. A clock enable signal LH2 is supplied on line 4638 to the register 4634. The source of the signal LH2 on line 4638 is the multiplexer 4639 which receives as input the CEN signal and V_{CC}.

The output of the register 4634 is supplied to line 4607, which drives the output Q2, and to line 4624, which is coupled as a first input to multiplexer 4640 and as an input to multiplexer 4622. The second input to multiplexer 4640 is the output Q1 of register.latch 4615 on line 4621. The third input to multiplexer 4640 is the signal O on line 4630.

The output of multiplexer 4640 is the pin output signal PO on line 4641. It is supplied through the tristate output buffer 4642 to the IO pad 4600. The tristate buffer includes a slew rate control circuit 4643 as known in the art. Further, a pass transistor 4644 and resistor 4645 provide a pull up path to V_{CC} at the output of buffer 4642. This pull up path is enabled in response to the passive pull up circuit 4646 which is implemented by a configuration memory cell.

The tristate buffer 4642 is controlled by the tristate output signal TO on line 4647. The signal is generated at the output of multiplexer 4648 which receives four inputs. The inputs include V_{CC}, GROUND, and a true and complement version of the signal OEN.

Control signals K, GK, and GR are supplied directly from the interconnect structure. The control signals IEN, CEN and OEN are supplied at the output of respective multiplexers 4650, 4651, and 4652, each of which receives two inputs from the general interconnect.

The signal on IEN gives the ability for dynamic control of the input path through the buffer 4627.

The signal on OEN gives the ability for dynamic control of the output path through the output buffer 4642.

The signal CEN can be used as a clock or as a clock enable signal.

The signals SL1 and SL2 are derived at the output of 3:1 multiplexers 4653 and 4654. Two of the inputs to the multiplexers 4653 and 4654 are derived from the interconnect structure as described below and the third is coupled to ground. The signal SL1 allows the input register of the IOB to be loaded with data either from the pad or from an adjacent counterclockwise complex IOB through QP1 or QP2. The signal SL2 allows the output register of the IOB to be loaded with data from either the output of MUX 4623 or from the next adjacent counterclockwise IOB through QP1 or QP2.

The input register.latch 4615 can be configured to operate either as a latch or a register, in response to a memory cell in the configuration memory. When the element operates as a register, data at the input D is transferred to the output Q on the rising edge of the clock signal K1 on line 4616. When the element operates as a latch, any data change at D is seen at Q while the signal K1 is high. When K1 returns to the low state, the output Q is frozen in its present state and any change on D will not affect the condition of Q.

The slew rate control circuit 4643 allows the output to either have a fast or a slow rise time subject to the state of the memory cell controlling that function.

Each of the multiplexers shown in Fig. 46 is controlled by a memory cell or cells in the configuration memory with the exception of multiplexers 4631 and 4611. These two multiplexers are controlled by the signals SL1 and SL2.

In operation, the input path receives a signal from the pad 4600 on line 4608 and passes it through buffer 4609 to generate the signal PI on line 4610. The signal PI is supplied as an input to the register load multiplexer 4611 which is controlled by the control signal SL1. The second input to the multiplexer 4611 is

the direct connections supplied as inputs EM1 through EM4, EN1 through EN4, FM1 through FM4, and FN1 through FN4 supplied from the outputs X1 through X4 of eight neighbor CLBs. In Fig. 50, the connection of next adjacent CLBs to the inputs FM1 through FM4 and FN1 through FN4 are shown. Thus, the connection X4 from CLB of row i-2 column j is coupled to the input FN1 of the CLB of row i in column j. Output X2 of CLB of row i-2 in column j is coupled to the input FM3. Output X1 of CLB of row i and column j+2 is coupled to the input FN2. Output X3 of CLB of row i column j+2 is coupled to the input FM4. The output X4 of CLB of row i+2 in column j is coupled to the input FM1 of the center CLB. The output X2 of row i+2 and column j is coupled to the input FN3 of the center CLB. The output X3 of the CLB of row i and column j-2 is coupled to the input FN4. Output X1 of the CLB of row i in column j-2 is coupled to the input FM2.

As shown in Fig. 51, the output X4 of the CLB in row i-1 and column is coupled to the input EN1 of the center CLB in row i and column j. Output X2 of the CLB in row i-1 and column j is coupled to the input EM3 in the center CLB. Output X1 of the CLB in row i and column j+1 is coupled to the input EN2 of the center CLB. The output X3 of the CLB in row i column j+1 is coupled to the input EM4.

The output X2 of the CLB in row i+1 and column is coupled to the input EN3. The output X4 of the CLB in row i+1 in column j is coupled to the input EM1. The output X3 of the CLB in row i and column j-1 is coupled to the input EN4. The output X1 in the CLB in row i, column j-1 is coupled to the input EM2.

Note that the structure shown in Figs. 50 and 51 illustrate that the CLBs in the center of the array are directly coupled to eight neighbor CLBs. Further, the interconnections allow for direction of data flow in any direction through the direct connect structure among CLBs.

In an alternative system having eight neighbor CLBs, the CLB at row i-1, column j+1; row i+1, column j+1; row i-1, column j-1; and row i+1 column j-1 could be connected in place the four outer CLBs shown in Figs. 50 and 51. This would provide eight neighbors with diagonal interconnection paths through the device. However, it is found that the ability to traverse a row or column with a direct connect structure provides for enhanced speed in transferring signals across the device.

Fig. 52 illustrates the connection of the outputs X1 through X4 on the center CLB in row i column j to the eight neighbor CLBs.

The output X4 of the CLB in the center is connected to the input FM1 of the CLB in row i-2, column j; the input EM1 of the CLB in row i-1, column j; the input EN1 of the CLB in row i+1, column j; and the input FN1 in the CLB of row i+2, column j.

The output X1 is coupled to the input FN2 of the CLB in row i, column j-2; the input EN2 in the CLB in row i, column j-1; the input EM2 in the CLB in row i, column j+1; and the input FM2 in the CLB in row i, column j+2. The output X2 is coupled to the inputs FN3 and EN3 in the CLBs in rows i-2 and i-1, column j, respectively, and to the inputs EM3 and FM3 in the CLBs of rows i+1 and i+2, of column j, respectively. Finally, the output X3 is coupled to the inputs FM4 and EM4 of the CLBs in row i columns j-2 and j-1, respectively, and to the inputs EN4 and FN4 in the CLBs of row i columns j+1 and j+2, respectively.

The direct connections on the peripheral CLBs which include direct connections to the IOBs are shown in Figs. 53-55. The figures are shown with the IOBs along the left side of the figure so that the columns of peripheral CLBs shown are columns 1 and 2. However, the connections apply as well for structures in which the peripheral CLBs are on rows 1 and 2 rather than columns 1 and 2, columns 7 and 8 rather than columns 1 and 2, and rows 7 and 8 rather than columns 1 and 2. The connections are just rotated where appropriate.

Furthermore, the connections of the CLBs in the corners are not shown. These CLBs can be connected up in a wide variety of configurations due to the converging nets at those corners. The specific direct connections of the corner CLBs and of all the other peripheral CLBs to IOBs on the array are shown in Table 1.

9	R1C3	FN1 FM3	X1
	R2C3	-	X1
10	R1C3	EN1	X2
	R2C3	FN1	X2
11	R1C4	EM3	X4
	R2C4	FM3	X4
12	R1C4	FN1 FM3	X1
	R2C4	-	X1
13	R1C4	EN1	X2
	R2C4	FN1	X2
16	R1C5	EM3	X4
	R2C5	FM3	X4
17	R1C5	FN1 FM3	X1
	R2C5	-	X1
18	R1C5	EN1	X2
	R2C5	FN1	X2
19	R1C6	EM3	X4
	R2C6	FM3	X4
20	R1C6	FN1 FM3	X1
	R2C6	-	X1
21	R1C6	EN1	X2
	R2C6	FN1	X2
22	R1C7	EM3	X4
	R2C7	FM3	X4
23	R1C7	FN1 FM3	X1
	R2C7	-	X1
24	R1C7	EN1	X2
	R2C7	FN1	X2
25	R1C8	EM3	X4
	R2C8	FM3	X4
26	R1C8	FN1 FM3	X1
	R2C8	-	X1

46	R6C8	EM4	X1
	R6C7	FM4	X1
47	R6C8	FN2 FM4	X2
	R6C7	-	X2
48	R6C8	EN2	X3
	R6C7	FN2	X3
49	R7C8	EM4	X1
	R7C7	FM4	X1
50	R7C8	FN2 FM4	X2
	R7C7	-	X2
51	R7C8	EN2	X3
	R7C7	FN2	X3
52	R8C8	EM4	X1
	R8C7	FM4	X1
53	R8C8	FN2 FM4	X2
	R8C7	-	X2
54	R8C8	EN2	X3
	R8C7	FN2	X3
57	R8C8	EM1	X2
	R7C8	FM1	X2
58	R8C8	FM1 FN3	X3
	R7C8	-	X3
59	R8C8	EN3	X4
	R7C8	FN3	X4
60	R8C7	EM1	X2
	R7C7	FM1	X2
61	R8C7	FM1 FN3	X3
	R7C7	-	X3
62	R8C7	EN3	X4
	R7C7	FN3	X4

80	R8C1	EM1	X2
	R7C1	FM1	X2
81	R8C1	FM1 FN3	X3
	R7C1	-	X3
82	R8C1	EN3	X4
	R7C1	FN3	X4
85	R8C1	EM2	X3
	R8C2	FM2	X3
86	R8C1	FM2 FN4	X4
	R8C2	-	X4
87	R8C1	EN4	X1
	R8C2	FN4	X1
88	R7C1	EM2	X3
	R7C2	FM2	X3
89	R7C1	FM2 FN4	X4
	R7C2	-	X4
90	R7C1	EN4	X1
	R7C2	FN4	X1
91	R6C1	EM2	X3
	R6C2	FM2	X3
92	R6C1	FM2 FN4	X4
	R6C2	-	X4
93	R6C1	EN4	X1
	R6C2	FN4	X1
94	R5C1	EM2	X3
	R5C2	FM2	X3
95	R5C1	FM2 FN4	X4
	R5C2	-	X4
96	R5C1	EN4	X1
	R5C2	FN4	X1

C1Ri is coupled directly to the EN1 and FN1 inputs of CLB in column 1 rows i + 1 and i + 2, respectively.

The output X1 in the CLB C2Ri is coupled directly to the O terminal of the complex IOB Ri1, and to the EN2 terminal of the CLB C1Ri. Output X1 is also coupled to the EM2 and FM2 inputs of CLBs C3Ri and C4Ri, respectively.

The output X2 of the CLB C2Ri is coupled directly to the inputs FN3 and EN3 of the CLBs C2Ri-2 and C2Ri-1. The output X2 of C2Ri is also coupled to the EM3 and FM3 inputs of CLBs C2Ri + 1 and C2Ri + 2.

The output X3 of the CLB C2Ri is coupled directly to the O terminal of the complex IOB Ri3, to the EM4 input of the CLB C1Ri to the EN4 input of CLB C3Ri and to the input FN4 of CLB C4Ri.

The output terminal X4 of the CLB C2Ri is connected directly to the inputs FM1 and EM1 of CLBs C2Ri-2 and C2Ri-1. Output X4 is also coupled to the inputs EN1 and FN1 of CLBs C2Ri + 1 and C2Ri + 2, respectively. In addition, the output X4 of CLB C2Ri is connected directly to the O terminal of the simple IOB Ri2.

The inputs EM1 through EM4 and EN1 through EN4 of the CLB C1Ri are shown in Fig. 54. The terminal EM1 is coupled to receive the output X4 of CLB C1Ri + 1. The input EN1 is coupled to receive the output X4 of the CLB CIRi-1. The input EM2 is coupled to receive an input from the complex IOB Ri3. The input EN2 is coupled to receive the output X1 of the CLB C2Ri. The input EM3 is coupled to receive the output X2 of the CLB C1Ri-1. The input EN3 is coupled to receive the output X2 of the CLB C1Ri + 1. The input EM4 is coupled to receive the output X3 of the CLB C2Ri. The input EN4 is coupled to receive an input from the complex IOB Ri1.

In Fig. 55, the FM1 through FM4 and FN1 through FN_4 inputs of CLBs C1Ri and C2Ri are shown.

The outputs X4 of CLBs C1Ri-2 and C2Ri-2 are connected respectively to the FN1 inputs of CLBs C1Ri and C2Ri. The outputs X2 of the CLBs C1Ri-2 and C2Ri-2 are connected directly to the inputs FM3 of CLBs C1Ri and C2Ri.

The outputs X1 of the CLBs C3Ri and C4Ri are connected directly to the FN2 inputs of CLBs C1Ri and C2Ri, respectively. The outputs X3 of the CLBs C3Ri and C4Ri are connected directly to the FM4 inputs of C1Ri and C2Ri.

The outputs X2 of the CLBs C1Ri + 2 and C2Ri + 2 are connected directly to the FN3 inputs of CLBs C1Ri and C2Ri, respectively. The outputs X4 of the CLBs C1Ri + 2 and C2Ri + 2 are connected directly to the FM1 inputs of CLBs C1Ri and C2Ri, respectively.

The terminal DS of the complex IOB Ri1 is coupled directly to the FN4 input of CLB C2Ri. The input DI received from the simple IOB Ri2 is coupled directly to the FN4 input and FM2 input of the CLB C1Ri. Finally, the input signal DI derived from the complex IOB Ri3 is coupled directly to the FM2 input of CLB C2Ri.

The programmable general connect is illustrated in Figs. 56-70. St provides a means for routing nets around the device. The CLBs and IOBs are linked through this network by means of programmable interconnection points PIPs. The programmable general connect is subdivided into the long lines and the bidirectional general interconnects BGI. which are lines incorporating metal segments spanning one or two CLBs, usually terminating in a switching matrix or segment box as described above with reference to Figs. 4-24.

The selection of the location of PIPs and their connection to the inputs and outputs of the configurable logic blocks and input/output blocks is a matter of design choice. The preferred implementation is shown as follows.

Fig. 56 shows the programmable connections of the outputs Y1 through Y4 to the long lines and BGI. The outputs Y1 through Y4 are also connected to the uncommitted long lines as shown in Fig. 58. Also, the outputs are coupled differently to the vertical bus 1 and horizontal bus 1, vertical bus 9 and horizontal bus 9 as shown in Fig. 59 as it relates to the long lines 1-4 in the respective buses.

Fig. 56 shows that the output Y1 is coupled to PIPs associated with long lines 3, 4, and 15, and BGIs 5, 9, 13, and 14 in HBUS i. The output Y2 of CLB CiRi is coupled to VBUS i + 1 long lines 1 and 2 and 15, and BGIs 5, 7, 11, and 14. Output Y3 of CiRi is coupled to HBUS i + 1 long lines 1, 2, and 15, and to BGI lines 5, 8, 12, and 14. The output Y4 of CiRi is coupled to VBUS i long lines 3, 4, and 15, and to BGI 5, 6, 10, and 14.

Also shown in Fig. 56 are the inputs to C1 through C4 and D1 through D4. These inputs are coupled as the unidirectional PIPs using four to one multiplexers in the preferred system to save on memory. One could use bidirectional PIPs, if desired.

The input C1 is coupled to BGI 7, 9, i11, and 13 on HBUS i. Input D1 is coupled to BGI 6, 8, 10, and 12 on HBUS i.

Input C2 is coupled to BGI of VBUS i + 1 lines 6, 8, 10, and 12, while input D2 is coupled to VBUS i + 1 BGI 7, 9, 11, and 13.

can be seen from the IOBs C4-1, C4-2, C4-3, C5-1, C5-2, and C5-3 at the top or bottom of the chip. These connections are similarly made for IOBs at the end of each column or row in the chip.

The four long lines 1-4 of each bus have a programmable pull up resistor at their ends (not shown). These four long lines are envisioned to be used for connectivity between the IOBs and CLBs in the center of the device, or long reach between CLBs. The pull up resistor can be enabled by the program data in the configuration memory such that if no signal arrives at the line, the line can be taken to a logical one state. This stops lines form carrying spurious signals across the whole device.

A second feature of the pull up is the ability to construct a wired-AND by driving the line from a number of CLBs or IOBs output buffers that are tristatable.

Each output buffer may be configured such that when passing a logic zero, the buffer asserts a low to the long line. When passing a logic 1, the buffer assertgs a tristate (high impedance) to the line. If no other buffer is driving the line (i.e. all buffers connected are in tristate - the logic 1 case for each) the the pull-up resistor forces a logic high onto the line, giving the result of the AND function required.

Figs. 61-70 show connections to the IOB structure with the interconnect. In Fig. 61, the connections of the input terminals I and the output terminals O of the eight groups of input/output blocks along the top side of the array to horizontal bus 1 are shown. In the figure, the circular symbols at the intersection of lines refer to bidirectional PIP connections. The squares at the intersection indicate a connection to the multiplexer in the IOB which generates the O signal which is described above with reference to Figs. 45 and 46. It can be seen upon review of Fig. 61 that each IOB input terminal I is coupled to one BGI and one uncommitted long line through a PIP. Each output terminal O in the IOBs is coupled to one uncommitted long line and one BGI at the input multiplexer. In addition, the input terminal I of the simple IOBs in respective centers of the triplets, are all coupled to long line 15 through a PIP. The distribution of the connections has been chosen to provide for a predictable scheme that facilitates programming of networks on the device. A wide variety of interconnection schemes could be implemented as meets the needs of a specific application.

Fig. 62 illustrates the connections to the IOBs along the bottom side to horizontal bus 9. The pattern of connections on Fig. 62 is similar to that of Fig. 61. The same explanation applies.

Fig. 63 shows the IOB connections along the left side of the array to vertical bus 1. Again, this connection scheme is similar to that as described with reference to Fig. 61 and the explanation is not restated.

Fig. 64 shows the IOB connections along the right side or the array to vertical bus 9. Again, this interconnection scheme is similar to that described with reference to Fig. 61 and is not explained again.

Figs. 65-68 show the connections of the IOBs along the top side of the array to the vertical buses VBUS i and VBUS i + 1, and show the inputs for the control signals GK, GR and K. Note that the input 1 of IOB Ci1 is coupled through a PIP to long line 3 of VBUS i in addition to the connections shown in Fig. 61. The terminal O of IOB Ci1 is coupled through the multiplexer inside the IOB to long line 4 of VBUS i. The GK and GR input signals are coupled to the long lines 16 and 17 of VBUS i. The input K is directly coupled to long line 15 of HBUS 1.

The simple IOB Ci2 has its terminal I connected through PIPs to long lines 3 and 15 of VBUS i, and long line 1 of VBUS i + 1. The terminal O on the simple IOB Ci2 receives as inputs to its multiplexer, connections to long line 2 of VBUS i + 1 and long line 4 of VBUS i.

The complex IOB Ci3 has its input terminal I coupled to long line 1 of VBUS i + 1 and a multiplexer generating the signal O coupled to receive the signal on long line 2 of VBUS i + 1. The control signals GK and GR in IOB Ci3 are coupled to long line 16 and 17 of VBUS i. Control input K is coupled to long line 15 of HBUS 1.

Fig. 66 shows connections to the IOBs along the bottom side with the vertical buses VBUS i and VBUS i + 1, as well as the control inputs K, GR, and GK. Note that the connections to these IOBs is similar to that described with reference to Fig. 65, except that the terminal I in the simple IOB Ci2 is connected to long line 4 of VBUS i and long lines 2 and 15 of VBUS i + 1. In this manner, the long line 15 of VBUS i + 1 is connected to receive signals from the simple IOB Ci2 along the bottom side of the array while the VBUS i line 15 is coupled to receive a signal from the IOB at the top side of the array for IOBs over one column of CLBs.

Fig. 67 shows connections to the IOBs along the left side of the array with the horizontal buses HBUS i and HBUS i + 1 and with the control signals supplied along VBUS 1.

The complex IOB Ri1 receives an input from long line 3 of HBUS i at its terminal O. The I terminal of Ri1 is coupled through a PIP to long line 4 of HBUS i. Control signals K, GR and GK are coupled to lines 15, 17, and 16 respectively of VBUS 1. The output O of simple IOB Ri2 is coupled to receive inputs from long line 3 of HBUS i and long line 1 of HBUS i + 1. The terminal I of simple IOB Ri2 is coupled through

do not suffer a speed penalty.

Overall, the present invention allows for implementation of a programmable gate array in which the symmetry of the interconnections, the ability to provide multi-source nets, the ability to propagate signals long distances across. the array without suffering speed penalty, and greater combinational logic capability are combined.

The present invention thus allows implementation of programmable gate arrays that are adaptable to a wider variety of applications than the prior art. Further, these implementations allow manufacture of a programmable gate array with greater functional density that can be efficiently utilized at a greater percentage capacity than available in prior art architectures for PGAs.

The foregoing description of preferred embodiments of the present invention has been provided for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise forms disclosed. Obviously, many modifications and variations will be apparent to practitioners skilled in this art. The embodiments were chosen and described in order to best explain the principles of the invention and its practical application, thereby enabling others skilled in the art to understand the invention for various embodiments and with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the following claims and their equivalents.

Claims

1. A configurable logic array, comprising:
configuration storage means for storing program data specifying a user defined data processing function;
a plurality of configurable logic means $CL_{c,r}$, arranged in an array consisting of C columns and R rows, where c designates a column in the range 1 to C, and r designates a row in the range 1 to R, each of the conf igurable logic means $CL_{c,r}$ having a plurality of inputs and outputs, and coupled to the configuration storage means, for generating cell output signals at the respective plurality of outputs in response to cell input signals supplied to the respective plurality of inputs and in response to program data in the configuration storage means;
a plurality of conf igurable input/output means, each coupled to an input/output pad and having an input and an output, and coupled to the configuration storage means, for providing configurable interfaces between the respective input/output pads and the respective inputs and outputs in response to program data in the configuration storage means;
configurable interconnect means, coupled to the plurality of configurable logic means, the plurality of configurable input/output means and the configuration storage means, for connecting inputs and outputs of configurable logic means and configurable input/output means into logical networks in response to program data in the configuration storage means;
wherein the configurable interconnect means is symmetrically disposed relative to the inputs and outputs of configurable logic means.

2. The configurable logic array of claim 1, wherein the configurable interconnect means includes
means for directly connecting one output of configurable logic means $CL_{c,r}$ to one input of sconfigurable logic means $CL_{c+2,r}$; and
means for directly connecting one output of configurable logic means $CL_{c,r}$ to one input of configurable logic means $CL_{c,r+2}$.

3. The configurable logic array of claim 1, wherein the configurable interconnect means includes a plurality of horizontal buses HB_i, for i equal to 1 to R + 1, along the rows in the array, and a plurality of vertical buses VB_j, for j equal to 1 to C + 1, along the columns of the array, so that each of the plurality of configurable logic means has four adjacent buses in the configurable interconnect means, and wherein each of the plurality of configurable logic means has at least one output coupled to each of the four adjacent buses.

4. The configurable logic array of claim 1, wherein the configurable interconnect means includes a plurality of horizontal buses HB_i, for i equal to 1 to R + 1, along the rows in the array, and a plurality of vertical buses VB_j, for j equal to 1 to C + 1, along the columns of the array, so that each of the plurality of configurable logic means has four adjacent buses in the configurable interconnect means, and wherein each of the plurality of configurable logic means has at least one input coupled to each of the four adjacent buses.

5. The configurable logic array of claim 1, wherein the configurable interconnect means includes a plurality of horizontal buses HB_i, for i equal to 1 to R + 1, along the rows in the array, and a plurality of vertical buses VB_j, for j equal to 1 to C + 1, along the columns of the array, so that each of the plurality of configurable logic means has four adjacent buses in the configurable interconnect means, and wherein each of the

the control line in a respective horizontal bus and to the first conducting line, for driving a signal from the control line in the respective horizontal bus to the first conducting line, or for driving a signal from the first conducting line to the control line in the respective horizontal bus, in response to program data in the configuration memory; and

a second plurality of configurable control line driving means, one for each vertical bus, and each coupled to the control line in a respective vertical bus and to the second conducting line, for driving a signal from the control line in the respective vertical bus to the second conducting line, or for driving a signal from the second conducting line to the control line in the respective vertical bus, in response to program data in the configuration memory.

10. The configurable logic array of claim 1, wherein the configurable interconnect means includes means for directly connecting one output of configurable logic means $CL_{c,r}$ to one input of configurable logic means $CL_{c+2,r}$;

means for directly connecting one output of configurable logic means $CL_{c,r}$ to one input of configurable logic means $CL_{c,r+2}$; and

means for directly connecting one output of configurable logic means $CL_{c,r}$ to one input of configurable logic means $CL_{c-2,r}$; and

means for directly connecting one output of configurable logic means $CL_{c,r}$ to one input of configurable logic means $CL_{c,r-2}$.

11. A configurable logic array, comprising:

configuration storage means for storing program data specifying a user defined data processing function;

a plurality of configurable logic means $CL_{c,r}$, arranged in an array consisting of C columns and R rows, where c designates a column in the row 1 to C, and r designates a row in the range 1 to R, each of the configurable logic means $CL_{c,r}$ having a plurality of inputs and outputs, and coupled to the configuration storage means, for generating cell output signals at the respective plurality of outputs in response to cell input signalsMsupplied to the respective plurality of inputs and in response to program data in the configuration storage means;

a plurality of configurable input/output means, each coupled to an input/output pad and having an input and an output, and coupled to the configuration storage means, for providing configurable interfaces between the respective input/output pads and the respective inputs and outputs in response to program data in the configuration storage means; and

configurable interconnect means, coupled to the plurality of configurable logic means, the plurality of configurable input/output means and the configuration storage means, for connecting inputs and outputs of configurable logic means and configurable input/output means into logical networks in response to program data in the configuration storage means;

wherein at least one of the configurable input/output means includes:

a tristate buffer means, having an output connected to the configurable interconnect means, supplying an output ssignal or presenting a high impedance state at its output in response to a tristate control signal; and

means for supplying the tristate control signal in response to program data in the configuration storage means.

12. The configurable logic array of claim 11, wherein each configurable input/output means in a subset of the plurality of configurable input/output means includes a storage element having an input and an output, and further including

means, coupled to the storage elements in the subset of configurable input/output means and to the configuration storage means, for connecting the output of the storage element in a first selected configurable input/output means in the subset to the input of the storage element in a second selected configurable input/output means in the subset in response to program data in the configuration storage means.

13. The configurable logic array of claim 11, wherein each configurable input/output means in a subset of the plurality of configurable input/output means includes a storage element having an input and an output, and further including:

means, coupled to the storage elements in the configurable input/output means in the suhset and to the sconfiguration storage means, for connecting the input of the storage element in a selected configurable input/output means in the subset to the configurable interconnect means, and for connecting the output of the storage element in the selected configurable input-output means in the subset to the configurable interconnect means, in response to program data in the configuration storage means.

14. The configurable logic array of claim 11, wherein each configurable input/output means in a subset of the plurality of configurable input/output means includes a storage element having an input and an output, and further including:

output connected to the data input of the first tristate buffer means, for selecting a signal from one of its plurality of inputs for supply to its output, its plurality of inputs including the output of the storage element and the adjacent input/output pad.

19. The configurable input/output means of claim 16, further including:

a storage element, having a data input, a clock input and an output, for storing data from its data input for supply to its output, in response to a clock signal at its clock input; and

means, coupled to the programmable interconnect, for supplying a signal to the data input of the storage element; and

wherein the second means for supplying includes a second selecting means, having a plurality of inputs and an output connected to the data input of the second tristate buffer means, for selecting a signal from one of its plurality of inputs for supply to its output, its plurality of inputs including the output of the storage element and the programmable interconnect.

20. A plurality of configurable input/output cells providing configurable interconnection between adjacent input/output pads and a configurable logic array including an array of configurable logical cells, a programmable interconnect, and a configuration memory storing program data for configuring logical networks in the configurable logic array, each cell in the plurality comprising:

array output means, having a data input and an output connected to the adjacent input/output pad, for supplying data from the data input to its output; and

first means, coupled to the programmable interconnect, for supplying a data signal to the data input of the array output means;

array input means, having a data input and an output connected to the programmable interconnect, for supplying data From the data input to its output;

second means, coupled to the adjacent input/output pad, for supplying a data signal to the data input of the array input means;

a first storage element, having a data input, a clock sinput and an output, for storing data from its data input for supply to its output, in response to a clock signal at its clock input; and

a second storage element, having a data input, a clock input and an output, for storing data from its data input for supply to its output, in response to a clock signal at its clock input;

third means, coupled to the programmable interconnect, for supplying a signal to the data input of the first storage element;

fourth means, coupled to the adjacent input/output pad, for supplying a signal to the data input of the second storage element; and

wherein the first means for supplying includes an array output selecting means, having a plurality of inputs and an output connected to the data input of the array output means, for selecting a signal from one of its plurality of inputs for supply to its output, its plurality of inputs including the output of the first storage element, the output of the second storage element and the programmable interconnect; and

the second means for supplying includes an array input selecting means, having a plurality of inputs and an output connected to the data input of the array input means, for selecting a signal from one of its plurality of inputs for supply to its output, its plurality of inputs including the output of the first storage element, the output of the second storage element and the adjacent input/output pad.

21. The configurable input/output cell of claim 20, wherein the configurable logic array further includes a second plurality of configurable input output cells, the configurable input/output cells in the second plurality each comprising:

first tristate buffer means, having a data input, a control input, and an output connected to the adjacent input/output pad, for buffering data from the data input to its output or presenting a high impedance state to its output in response to a tristate control signal from the control input; and

a first programmable interconnect point, coupled to the control input of the first tristate buffer means and to the programmable interconnect, for supplying the tristate control signal in response to program data in the configuration memory;

first means, coupled to the programmable interconnect, for supplying a data signal to the data input of the first tristate buffer means;

second tristate buffer means, having a data input, a control input, and an output connected to the programmable interconnect, for buffering data from the data input to its output or presenting a high impedance state to its output in response to a second tristate control signal from the control input;

a second programmable interconnect point, coupled to the control input of the second tristate buffer means and to the programmable interconnect, for supplying the second tristate control signal in response to program data in the configuration memory; and

second means, coupled to the adjacent input/output pad, for supplying a data signal to the data input of the

supplying the selected element output signal as output on one line of the one bus or presenting a high impedance state in response to the output enable signal; and

a direct output buffer receiving a selected element output

31. A configurable logic element coupled to a configuration memory including a plurality of storage elements storing program data specifying a user defined data processing function, comprising:

input means for supplying a set of K input signals;

multiplexing means; coupled to the input means and a first set of storage elements in the configuration memory, for selecting a set of P signals and a set of Q signals from the first set of storage elements, in response to a first subset of the set of K input signals;

special output means, coupled to the multiplexing means and a second set of storage elements in the configuration memory, for selecting a special output signal from the second set of storage elements in response to the set of Q signals;

output means, coupled to the multiplexing means and the special output means, for selecting a first subset from the set of P signals and the special output signal, as element output signals.

32. The configurable logic element of claim 31, wherein the configurable logic element has a first side coupled with a first bus, a second side coupled with a second bus, a third side coupled with a third bus, and a fourth side coupled with a fourth bus, and wherein the input means includes:

means, coupled to the first, second, third and fourth buses and to the configuration memory, for selecting the first subset of the set of K input signals from signals on selected lines on the first, second, third and fourth buses in response to the program data in the configuration memory.

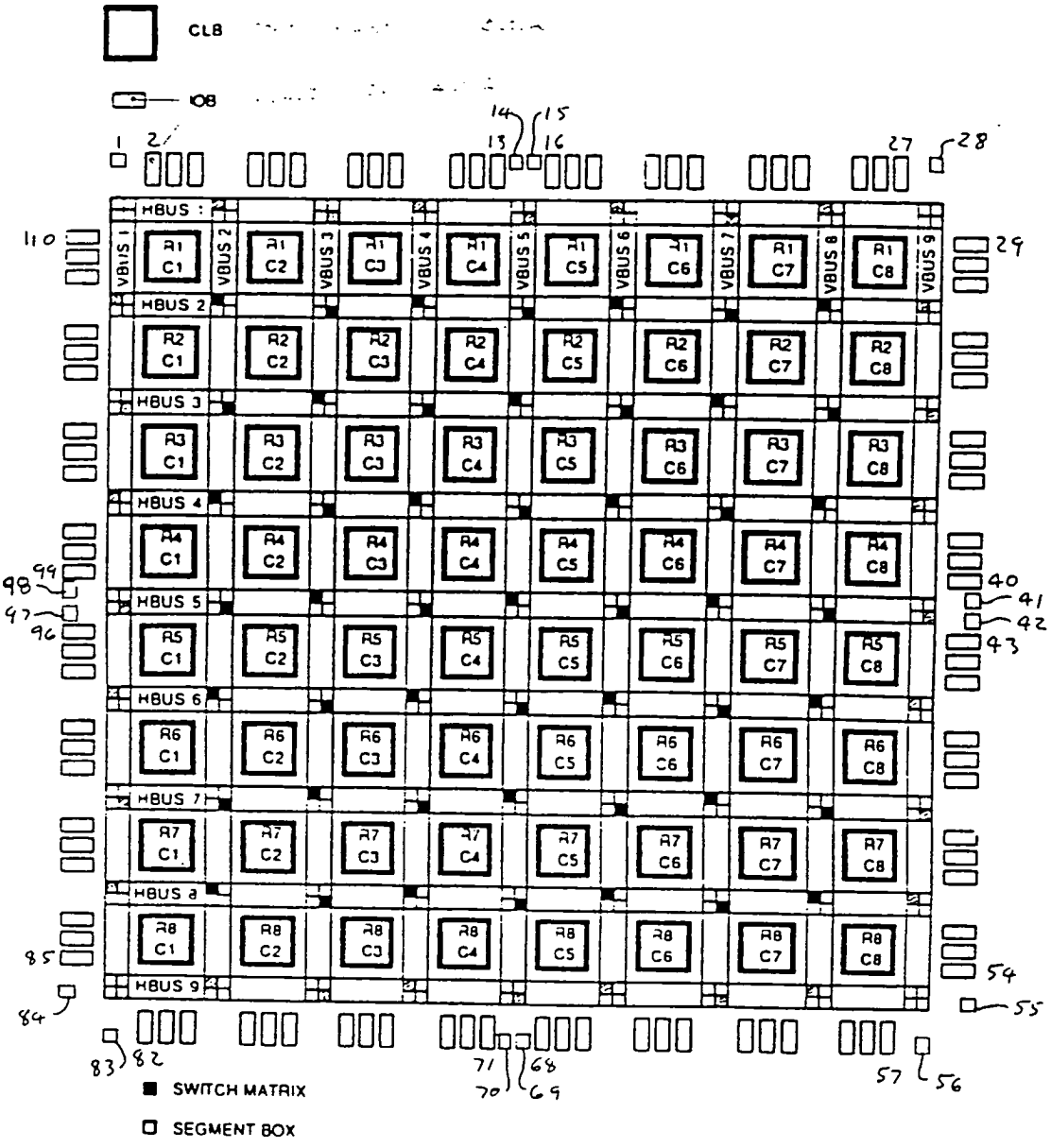

CLB
IOB
HBUS 1
HBUS 2
HBUS 3
HBUS 4
HBUS 5
HBUS 6
HBUS 7
HBUS 8
HBUS 9
VBUS 1
VBUS 2
VBUS 3
VBUS 4
VBUS 5
VBUS 6
VBUS 7
VBUS 8
VBUS 9
SWITCH MATRIX
SEGMENT BOX

FIG.-1

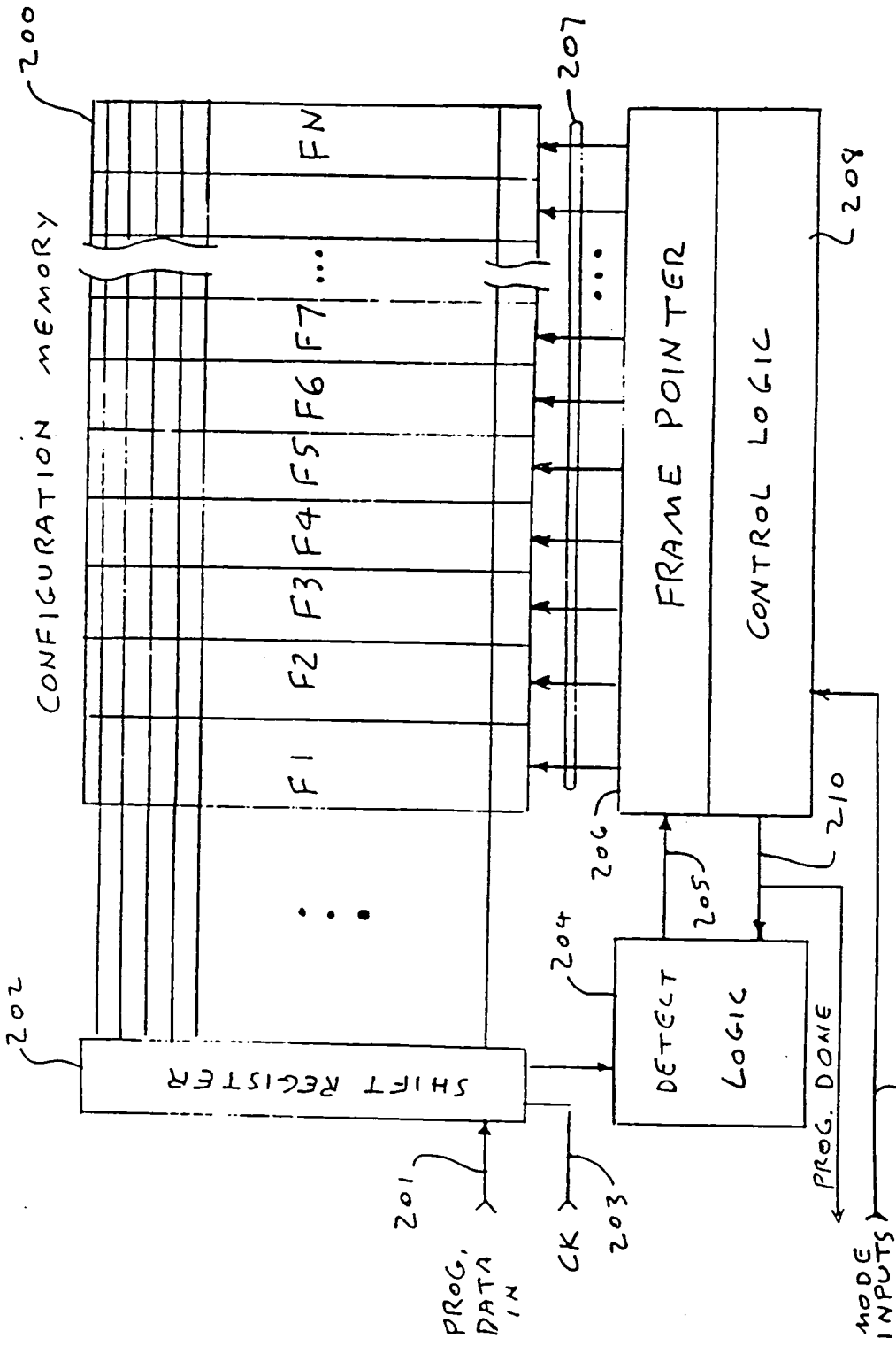

200
CONFIGURATION MEMORY
F1
F2
F3
F4
F5
F6
F7
FN
207
208
FRAME POINTER
CONTROL LOGIC
206
205
210
204
DETECT LOGIC
202
SHIFT REGISTER
201
PROG. DATA IN
CK
203
PROG. DONE
209
MODE INPUTS

FIG. - 2

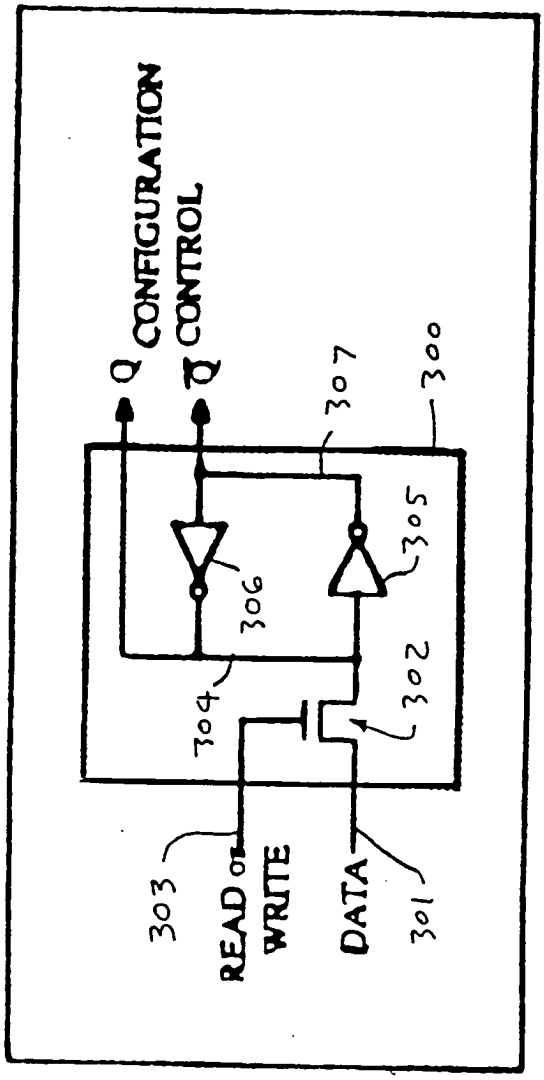
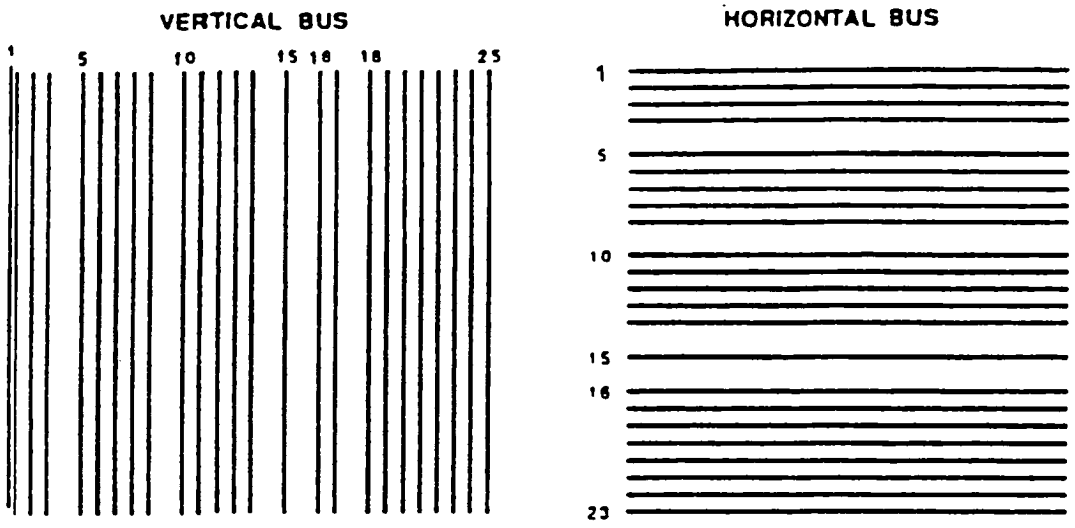

Q CONFIGURATION CONTROL
$\overline{Q}$
307
300
305
306
304
302
303
READ or WRITE
DATA
301

FIG.-3

NOTATION FOR BUSES 1 TO 9



VERTICAL BUS	
1	LONG LINE
2	LONG LINE
3	LONG LINE
4	LONG LINE
5	BIDIRECTIONAL GENERAL INTERCONNECT
6	
7	
8	
9	
10	
11	
12	
13	
14	
15	LONG LINE
16	CK
17	CR
18	UNCOMMITTED LONG LINES
19	
20	
21	
22	
23	
24	
25	

FIG. – 4

HORIZONTAL BUS	
1	LONG LINE
2	LONG LINE
3	LONG LINE
4	LONG LINE
5	BIDIRECTIONAL GENERAL INTERCONNECT
6	
7	
8	
9	
10	
11	
12	
13	
14	
15	LONG LINE
16	UNCOMMITTED LONG LINES
17	
18	
19	
20	
21	
22	
23	

FIG. – 5

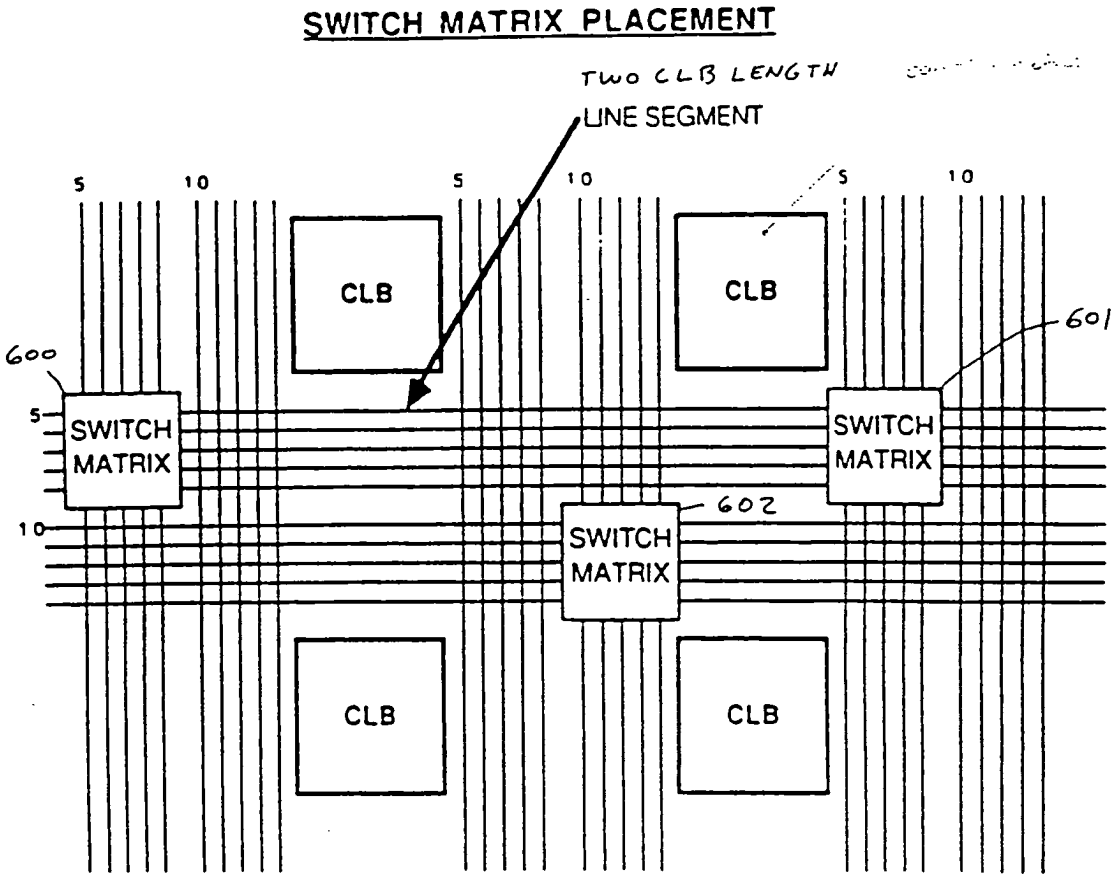

SWITCH MATRIX PLACEMENT
TWO CLB LENGTH
LINE SEGMENT
5
10
5
10
5
10
CLB
CLB
600
601
SWITCH MATRIX
SWITCH MATRIX
602
SWITCH MATRIX
CLB
CLB

FIG.-6

VERTICAL BUSES 2 to 8 TO HORIZONTAL BUSES 2 to 8 INTERCONNECT

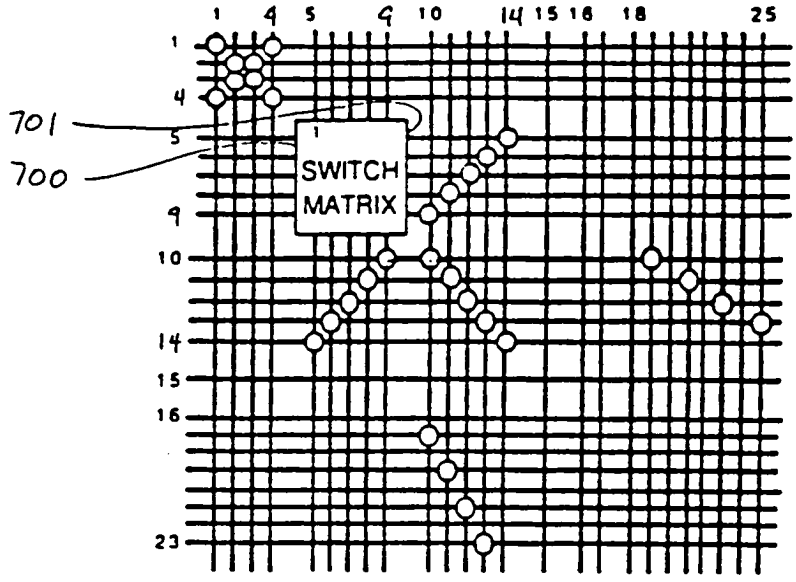


FIG.-7

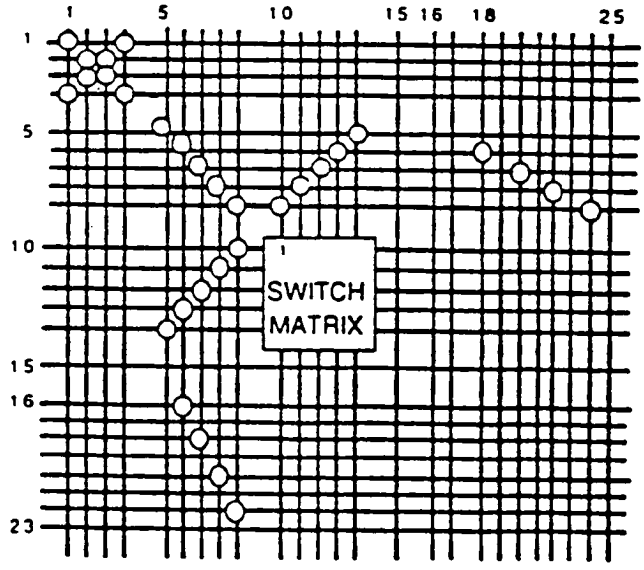


FIG.-8

SEGMENT BOX PLACEMENT ON BUSES 1 & 9

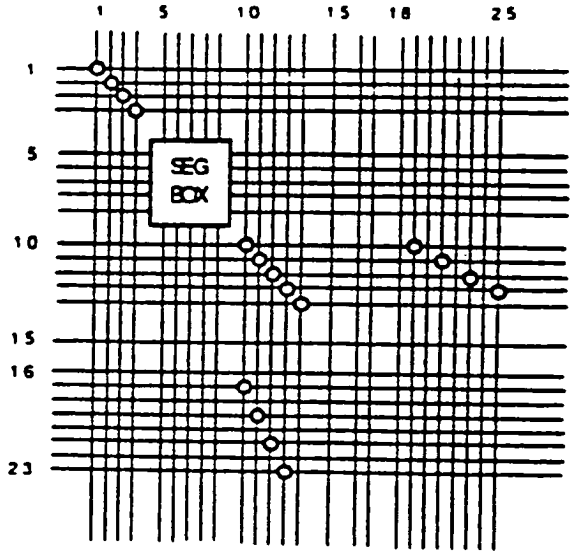


FIG.-9

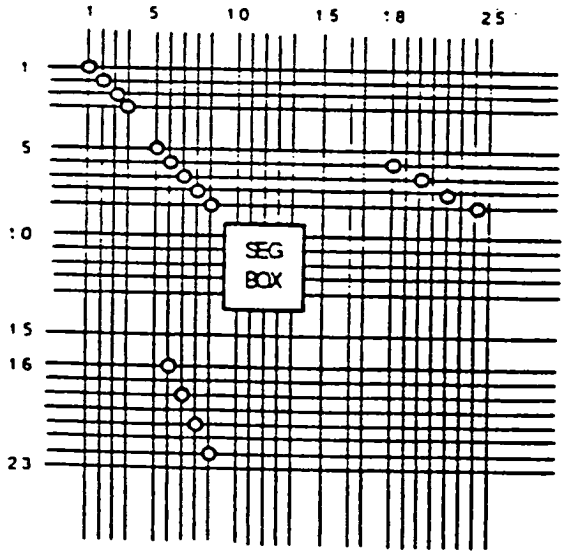


FIG.-10

CORNER INTERCONNECTS

HBUS1 TO VBUS1 INTERCONNECT

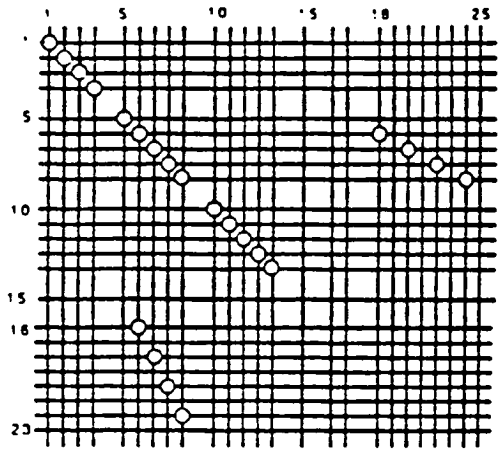


FIG.—11

HBUS1 TO VBUS9 INTERCONNECT

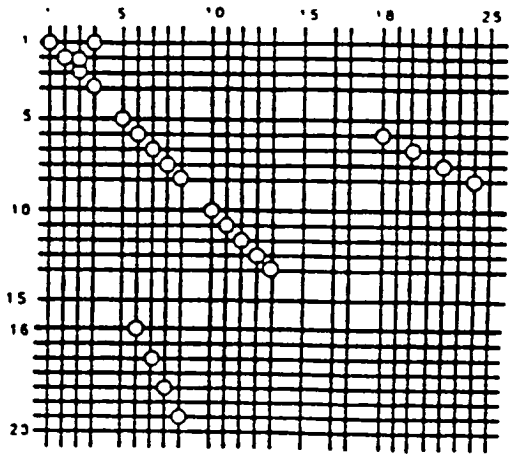


FIG.—12

HBUS9 TO VBUS1 INTERCONNECT

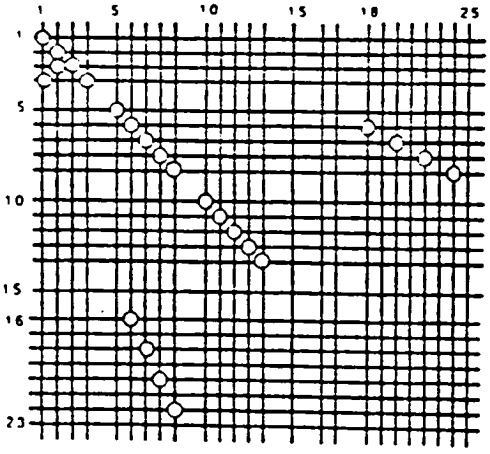


FIG.—13

HBUS9 TO VBUS9 INTERCONNECT

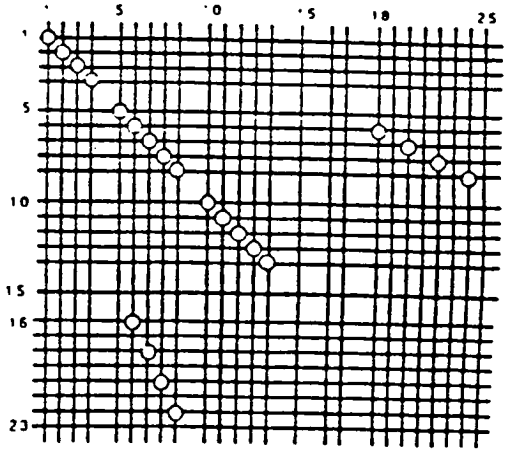
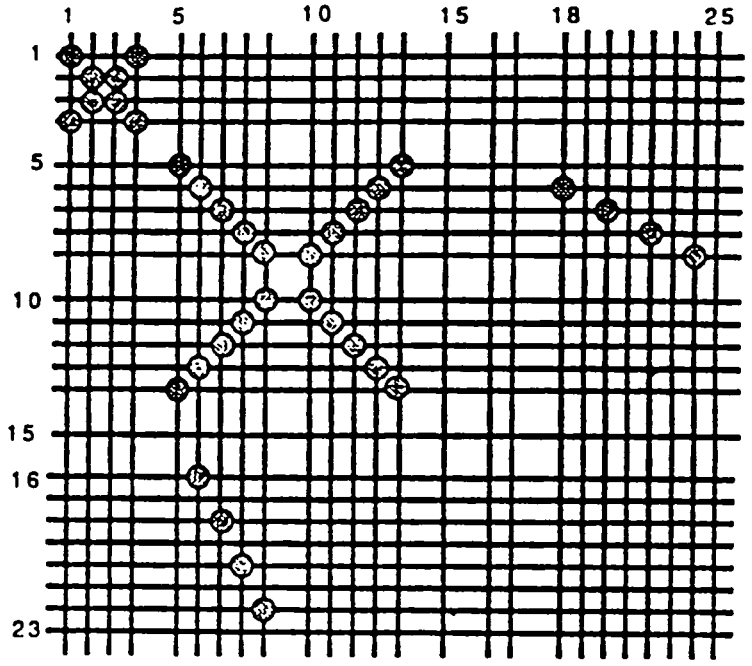


FIG.—14



A corner intersection of peripheral buses

FIG. 14A

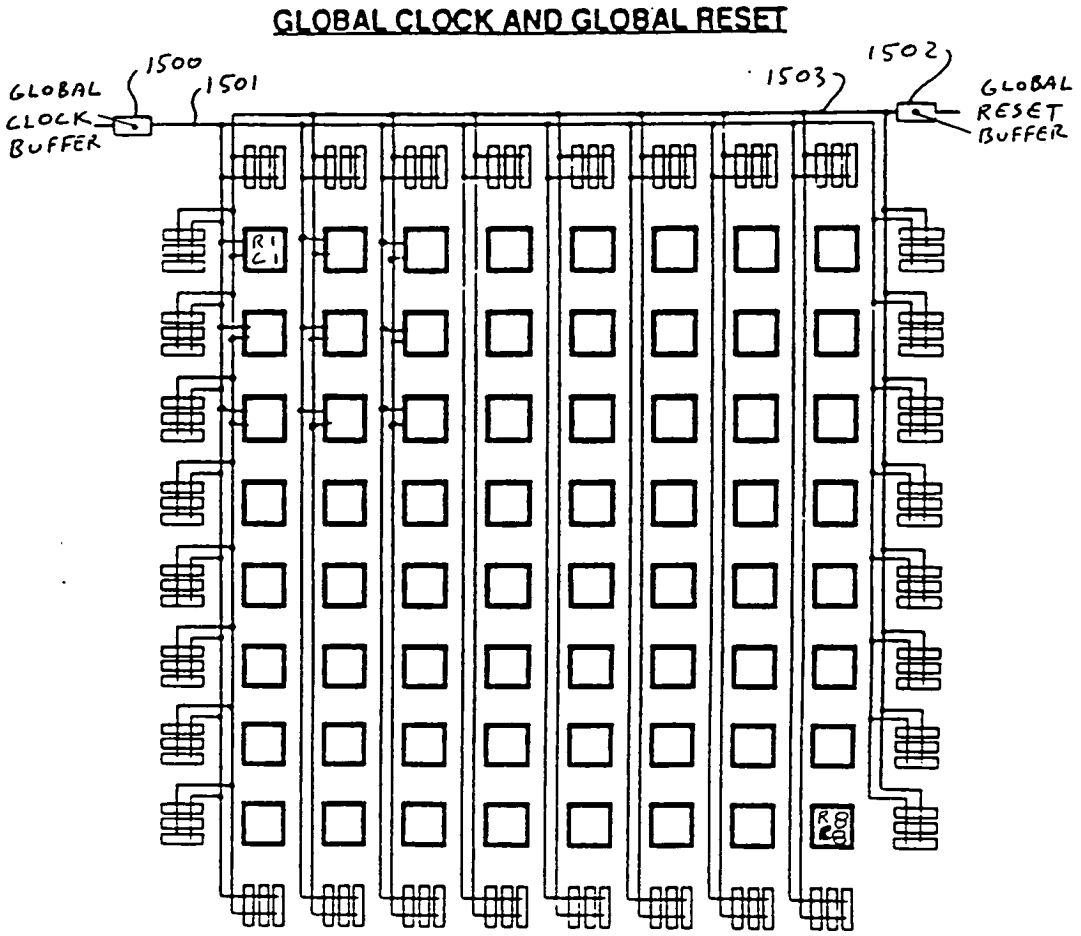


FIG.-15

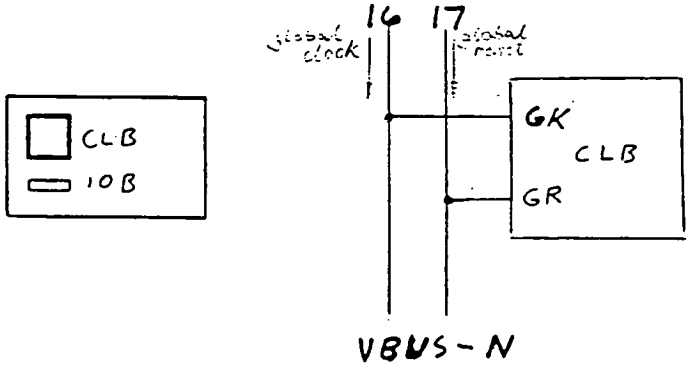
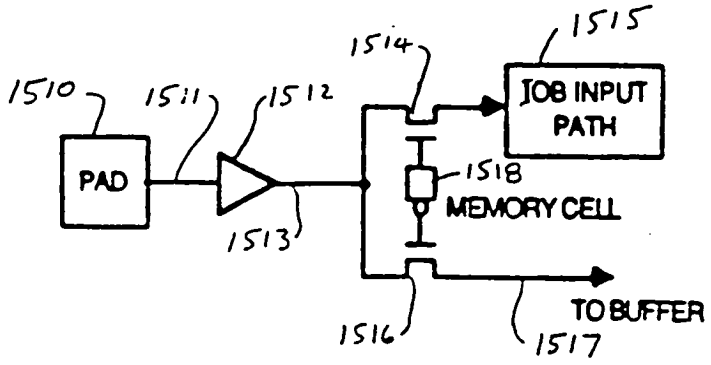
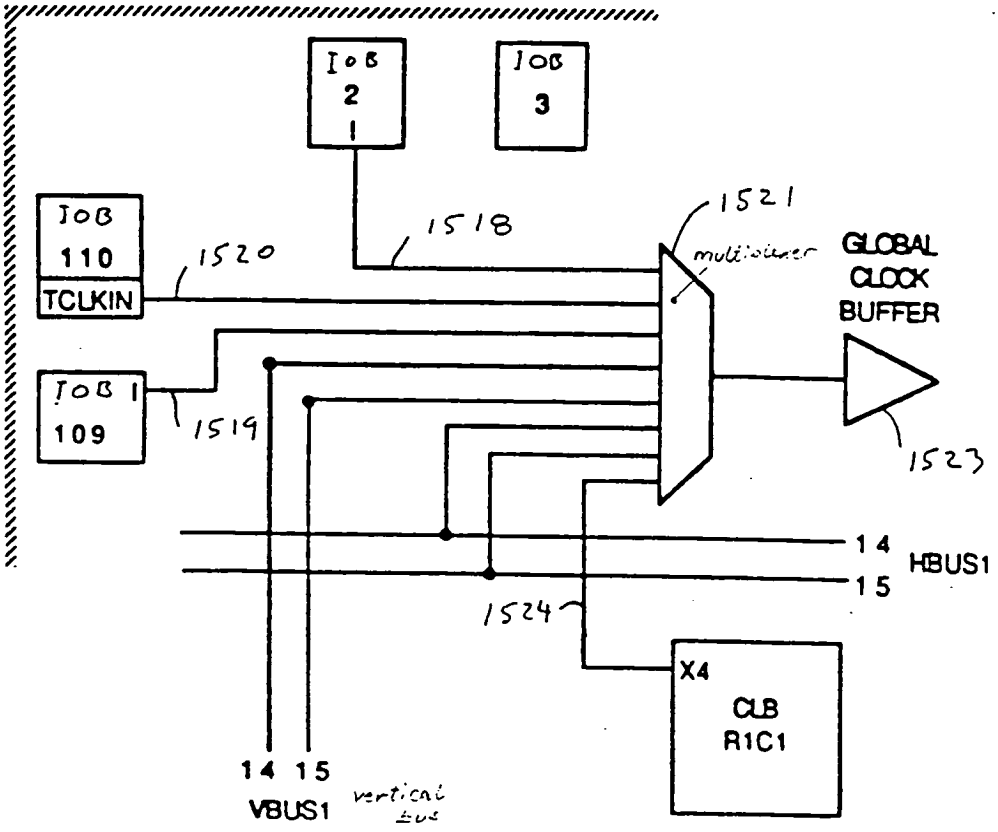


FIG.-15A



Special input to global buffers

FIG.—15B



Inputs to the Global Clock Buffer

FIG.—15C

ALTERNATE GLOBAL BUFFERS

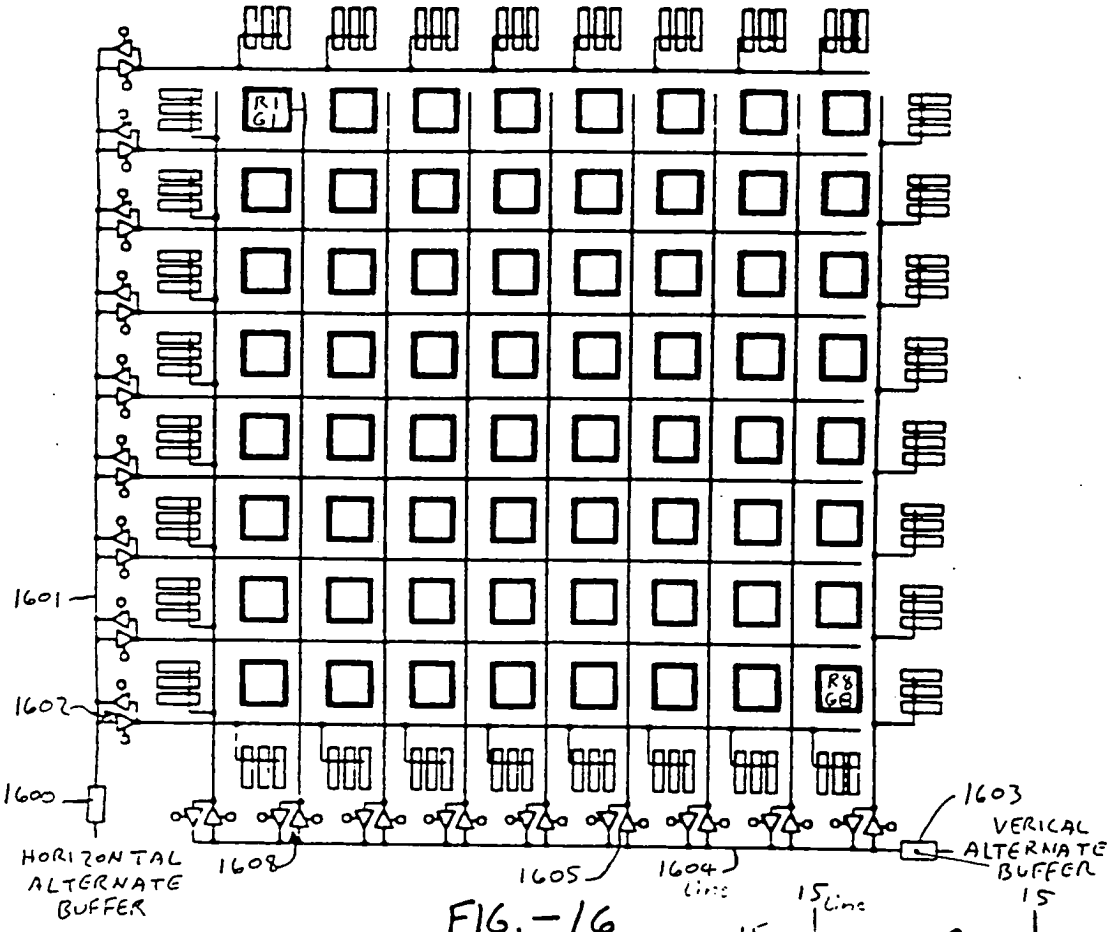
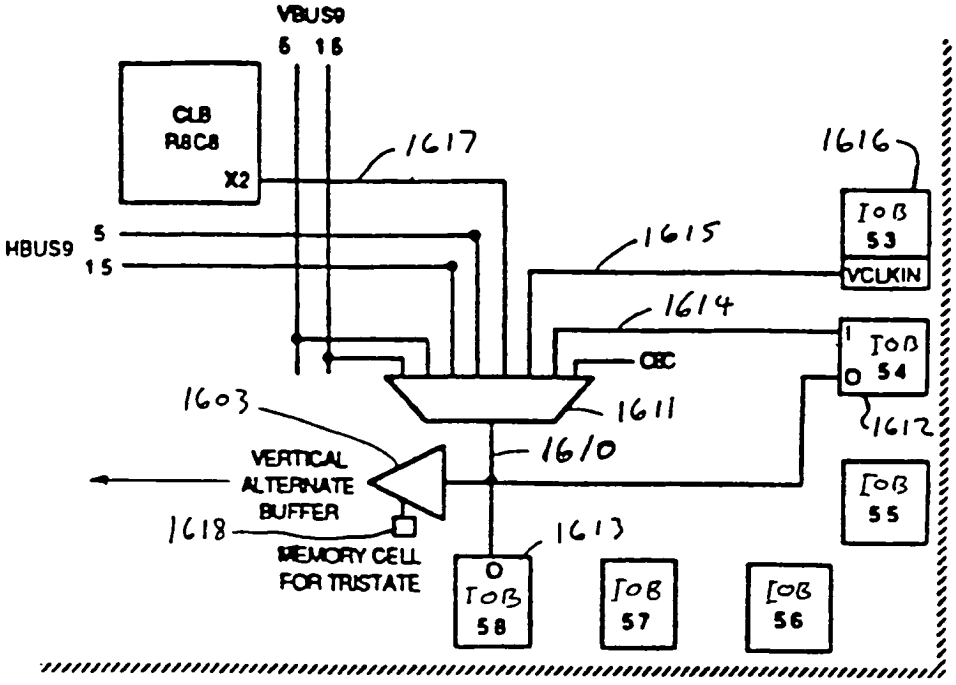


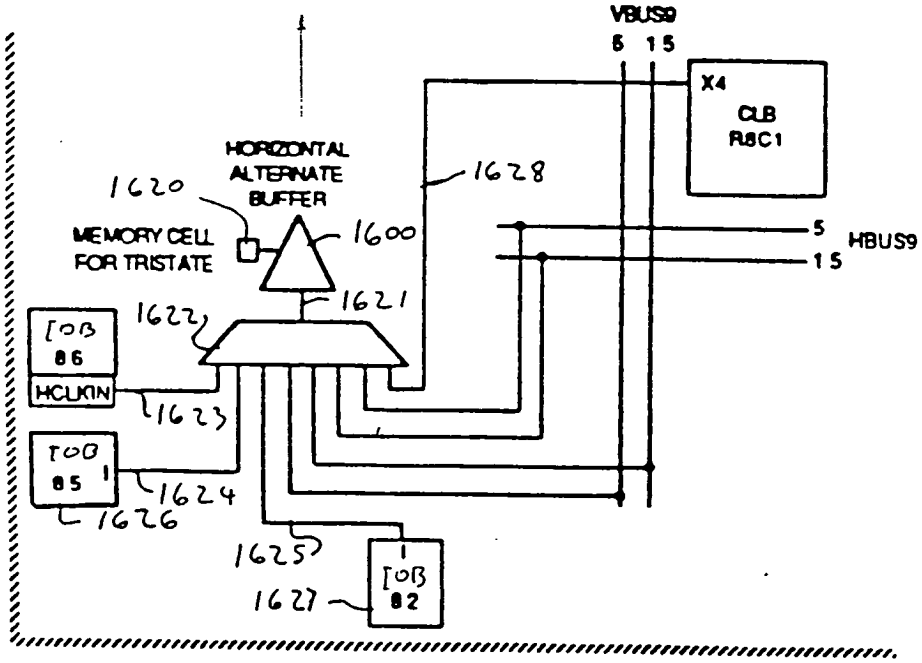
FIG.-16

FIG.-16A



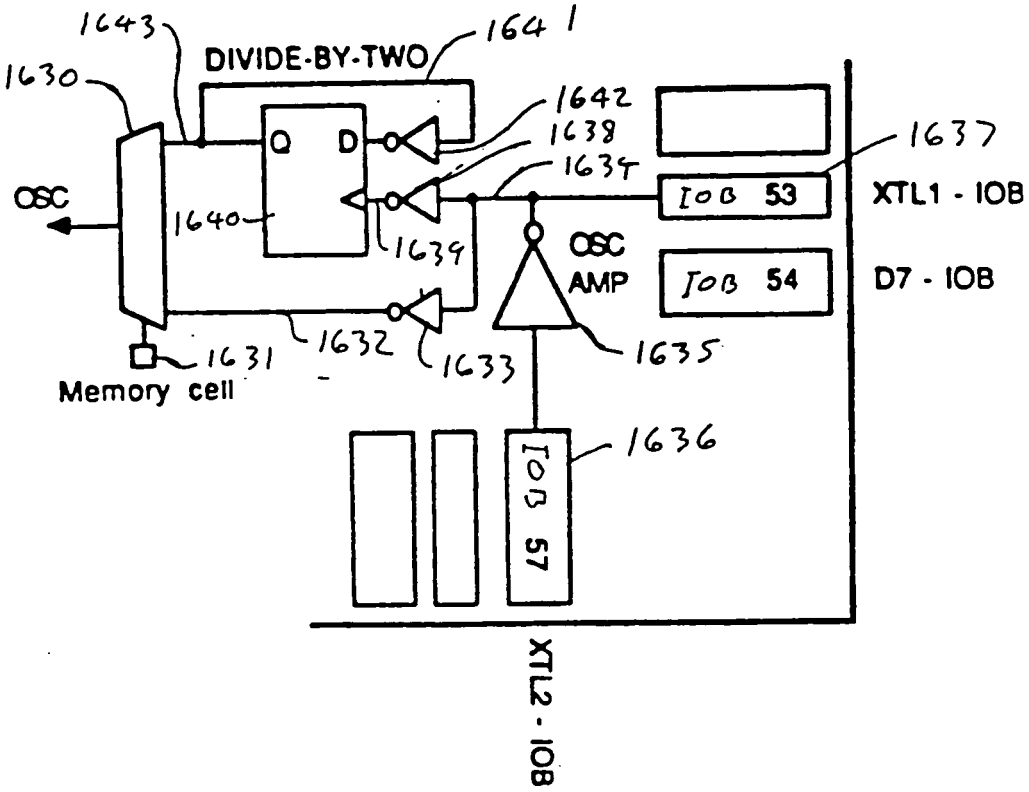
Inputs to the Vertical Alternate Buffer

FIG.-16B



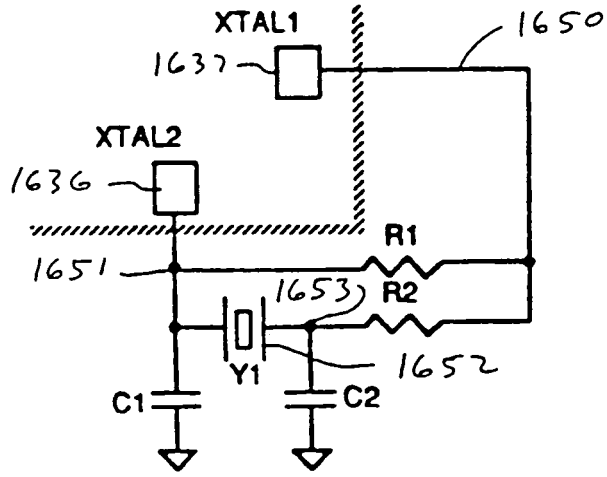
Inputs to the Horizontal Alternate Buffer

FIG.-16C



Crystal oscillator

FIG.-16D



Crystal components

FIG.-16E

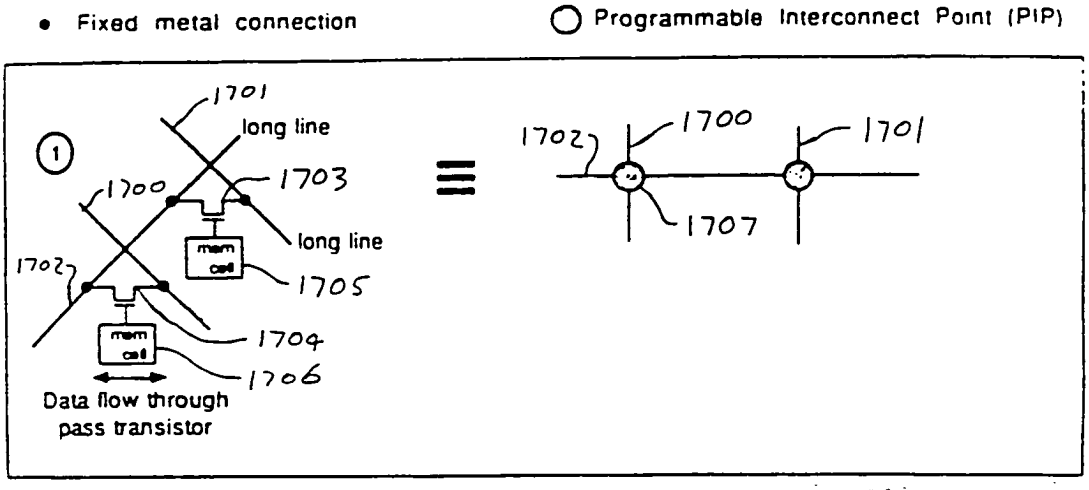

• Fixed metal connection
○ Programmable Interconnect Point (PIP)
1
1701
long line
1703
1700
long line
1702
mem cell
1705
1704
1706
Data flow through pass transistor
1702
1700
1701
1707

FIG. – 17

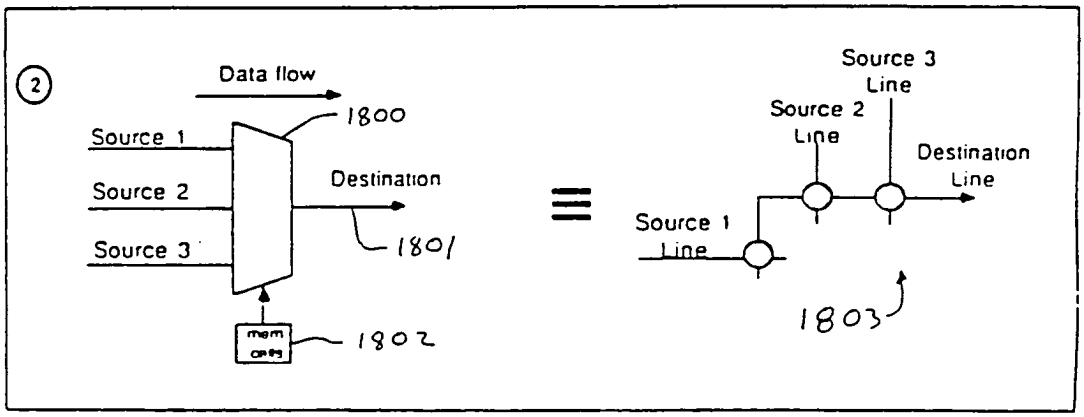

2
Data flow
1800
Source 1
Source 2
Source 3
Destination
1801
mem cells
1802
Source 3 Line
Source 2 Line
Destination Line
Source 1 Line
1803

FIG.-18

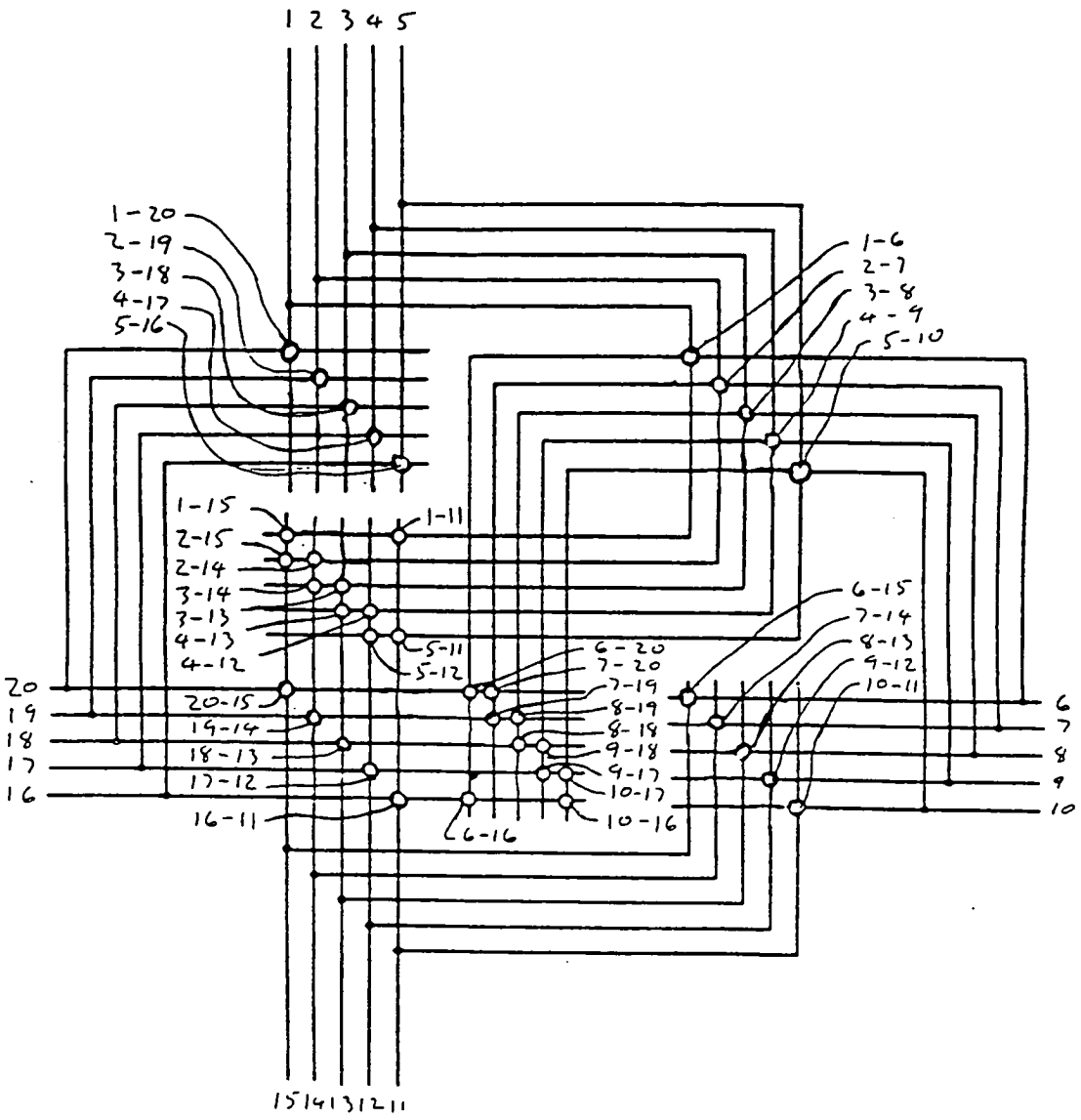
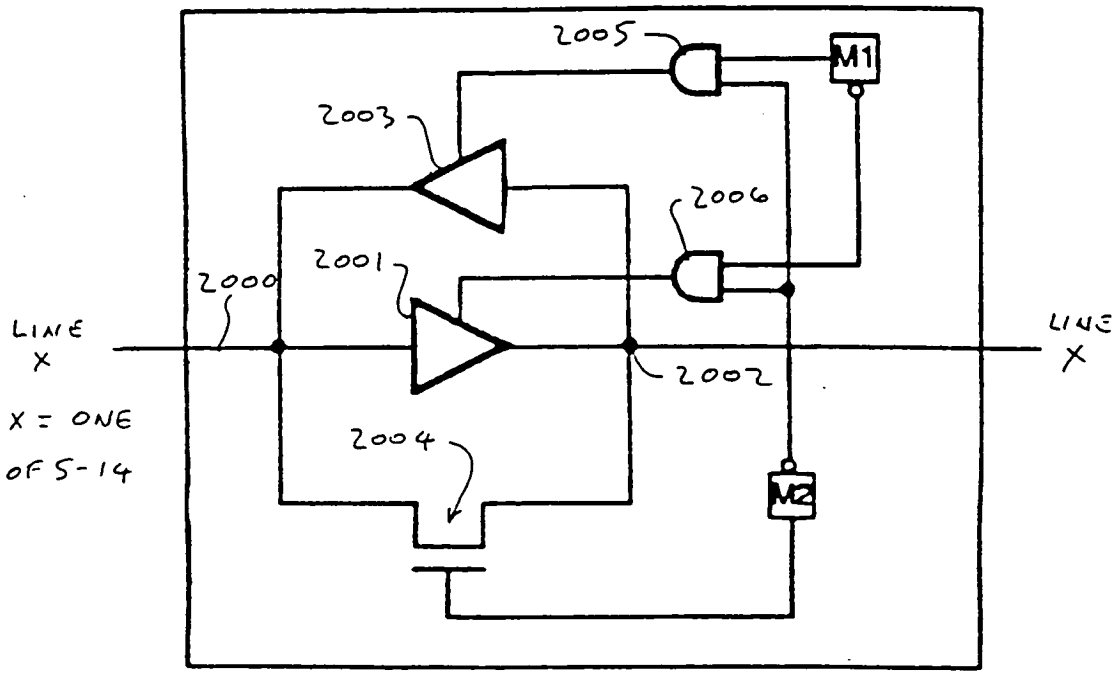

4000 SWITCH MATRIX
1 2 3 4 5
1-20
2-19
3-18
4-17
5-16
1-6
2-7
3-8
4-9
5-10
1-15
2-15
2-14
3-14
3-13
4-13
4-12
1-11
5-11
5-12
6-20
7-20
7-19
8-19
8-18
9-18
9-17
10-17
10-16
6-16
6-15
7-14
8-13
9-12
10-11
20-15
19-14
18-13
17-12
16-11
20
19
18
17
16
6
7
8
9
10
15 14 13 12 11

FIG.—19



REPOWERING: BUFFER

FIG. - 20

SWITCH MATRIX INTERCONNECTION OPTIONS FOR EACH TERMINAL

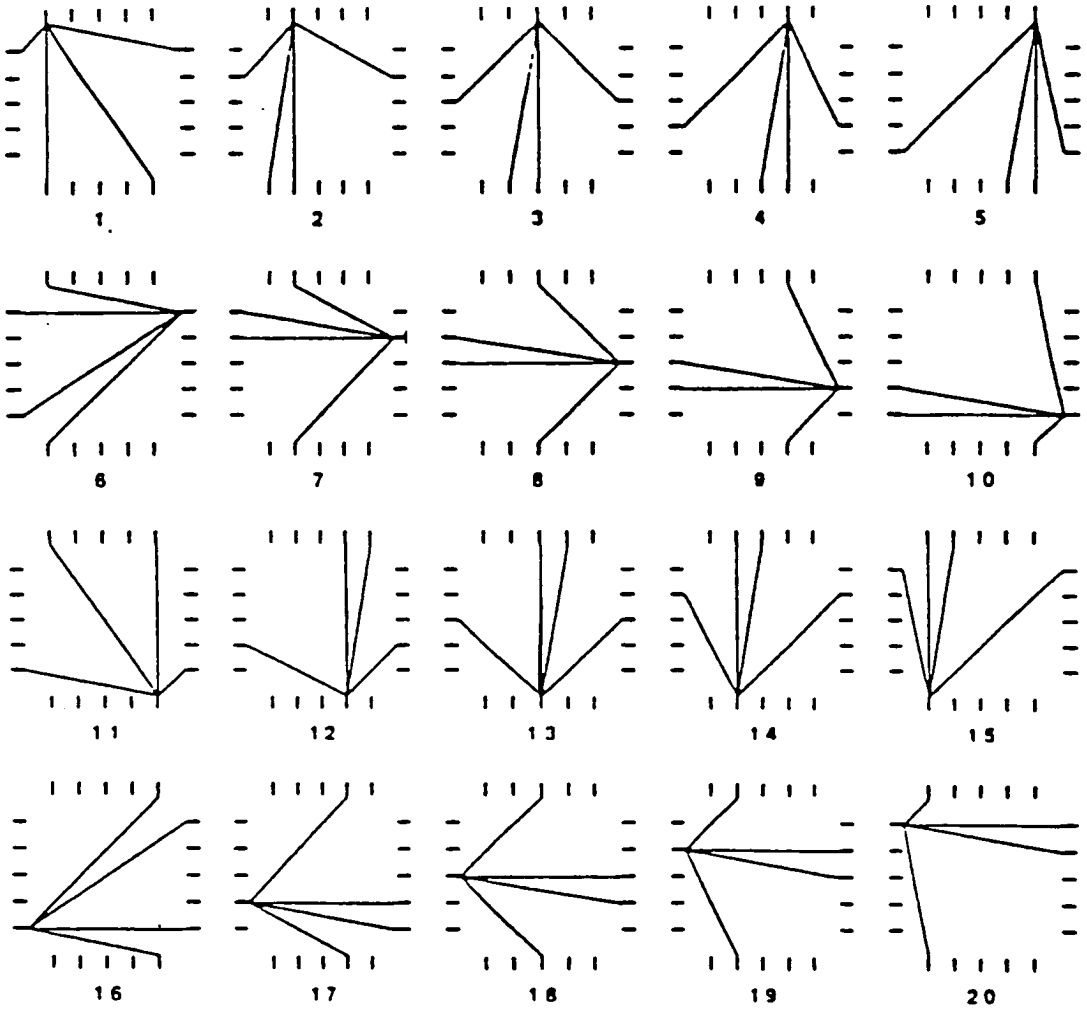


FIG. — 21

OUTER BUS SEGMENT BOXES

VERTICAL SEGMENT BOX

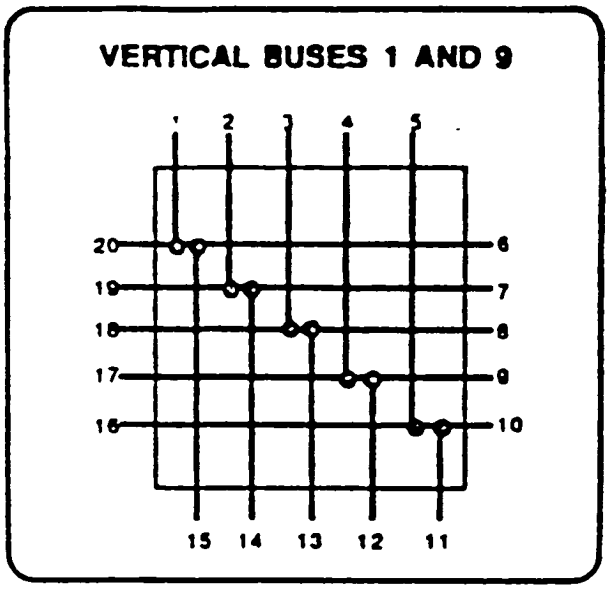


FIG.-22

HORIZONTAL SEGMENT BOX

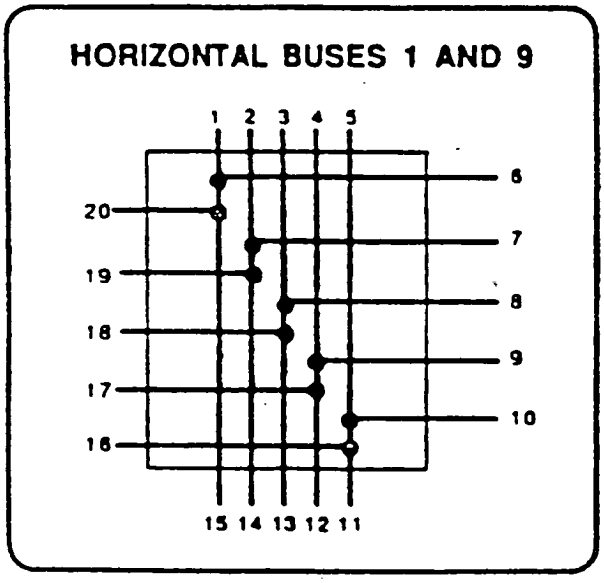


FIG.-23

SEGMENT BOX INTERCONNECTIONS FOR EACH PIN

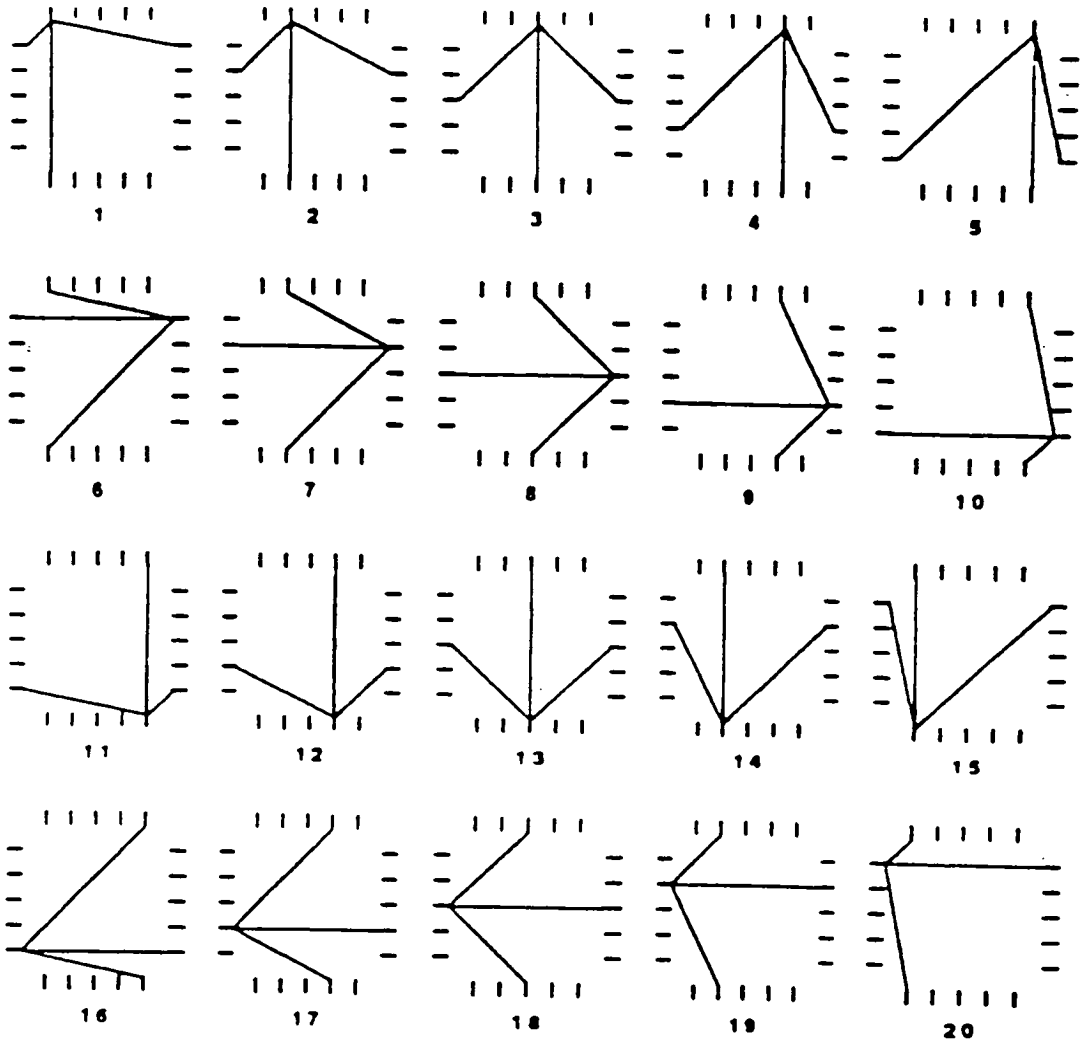


FIG.-24

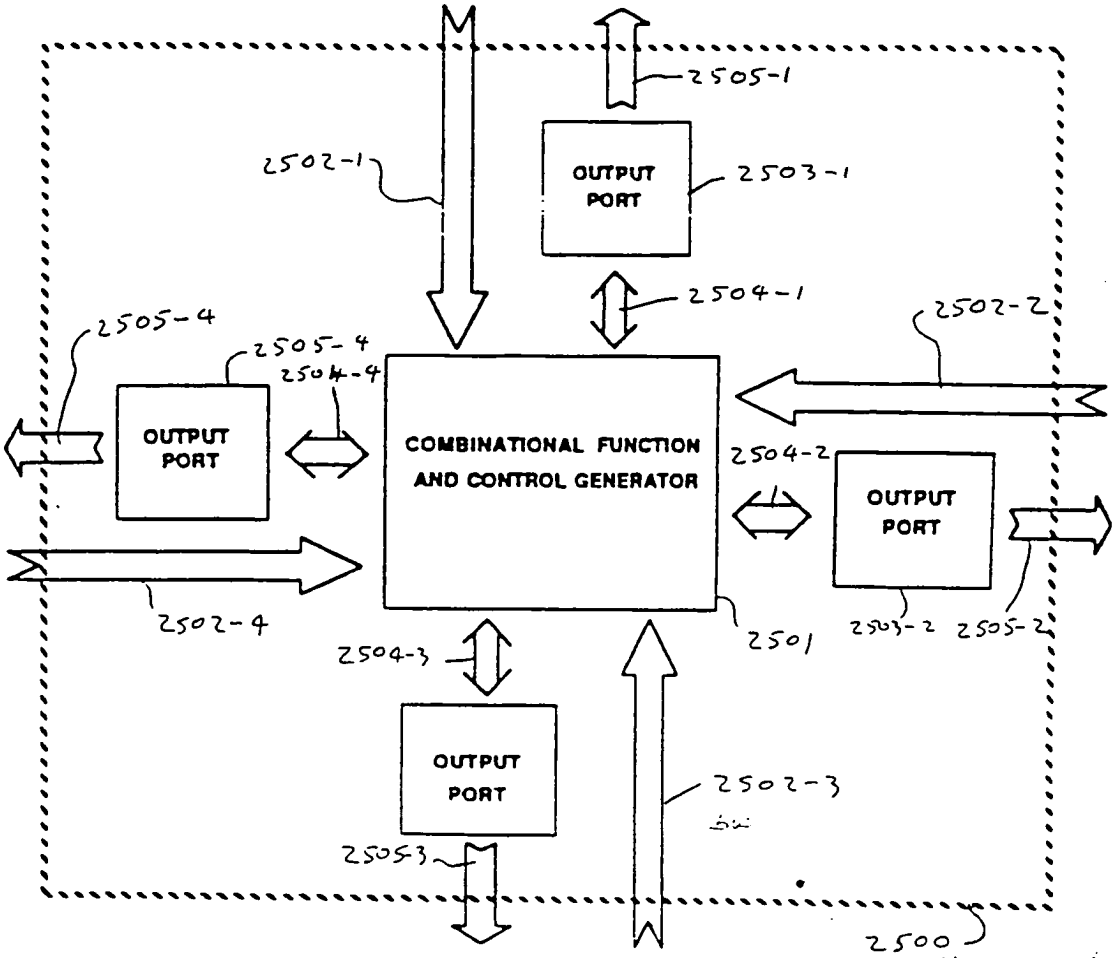
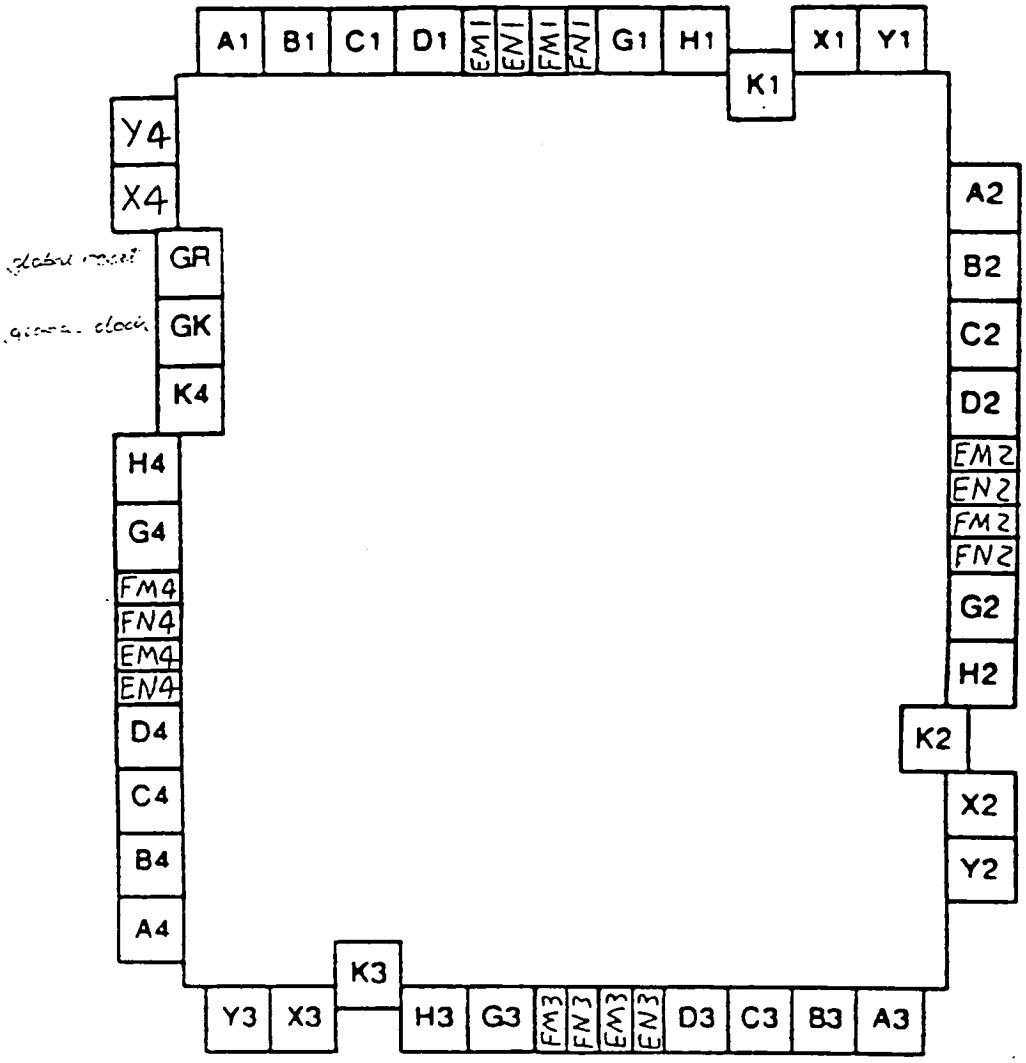

2505-1
2502-1
OUTPUT PORT
2503-1
2504-1
2505-4
2505-4
2504-4
2502-2
OUTPUT PORT
COMBINATIONAL FUNCTION AND CONTROL GENERATOR
2504-2
OUTPUT PORT
2502-4
2504-3
2501
2503-2
2505-2
OUTPUT PORT
2502-3
25053
2500

FIG. - 25

CONFIGURABLE LOGIC BLOCK NOTATION



A1 - A4 and B1 - B4	LONG LINE INPUTS
C1 - C4 and D1 - D4	GENERAL INPUTS (LOGIC)
EM1-EM4, EN1-EN4 and FM1-FM4, FN1-FN4	DIRECT CONNECT INPUTS
G1 - G4 and H1 - H4	GENERAL INPUTS (CONTROL)
K1 - K4	LONG LINE INPUT (BUS LINE 15)
X1 - X4	OUTPUT FOR DIRECT CONNECT
Y1 - Y4	OUTPUT TO GENERAL INTERCONNECT

FIG.-26

CLB CONFIGURATION

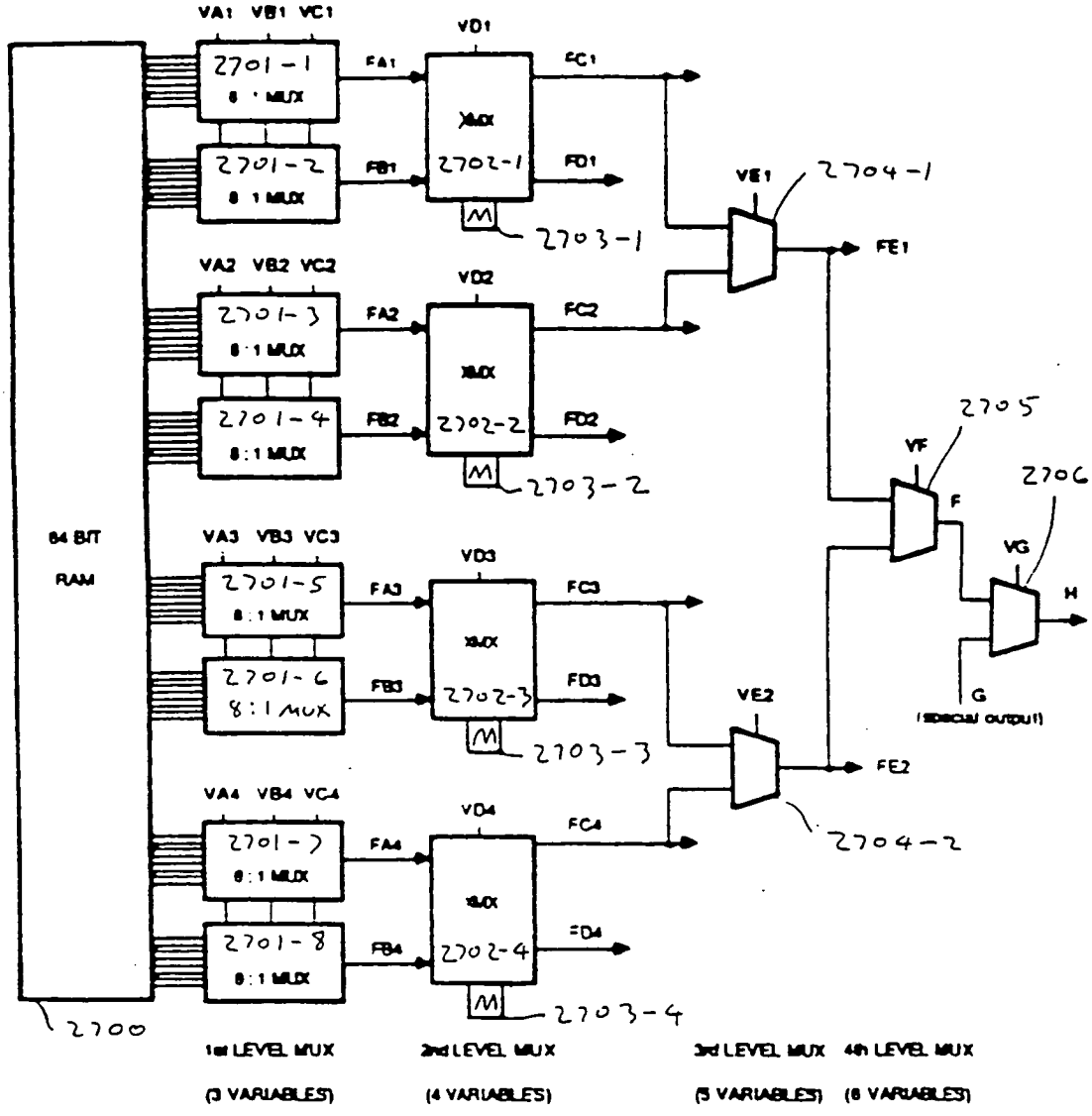
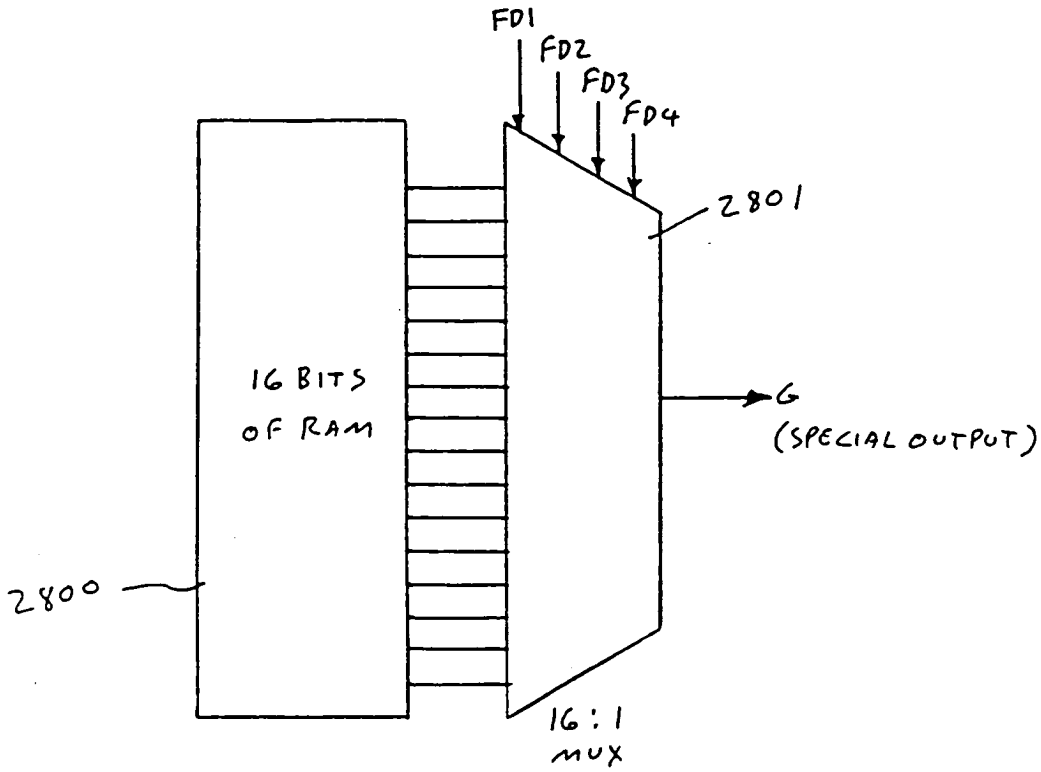


FIG.—27



SPECIAL OUTPUT STAGE

FIG - 28

CLB MACROCELLS

MACROCELL 1

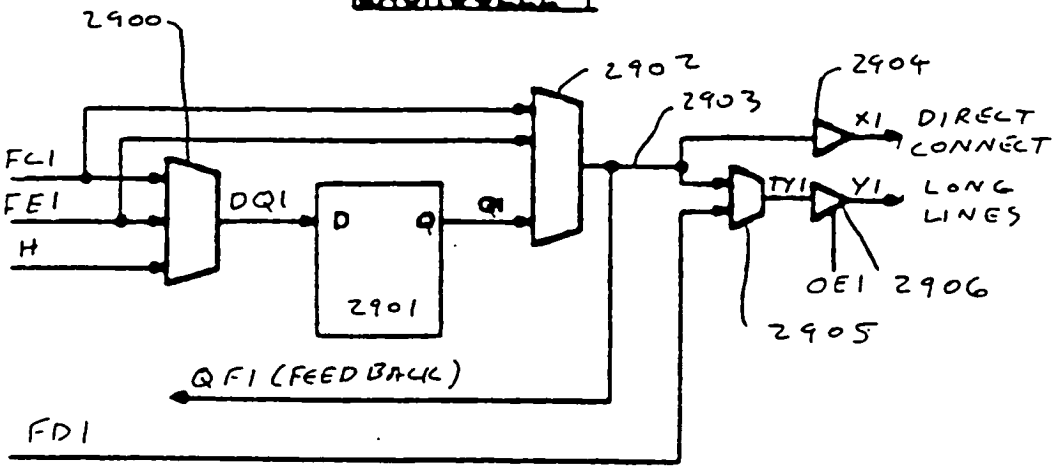


FIG.-29

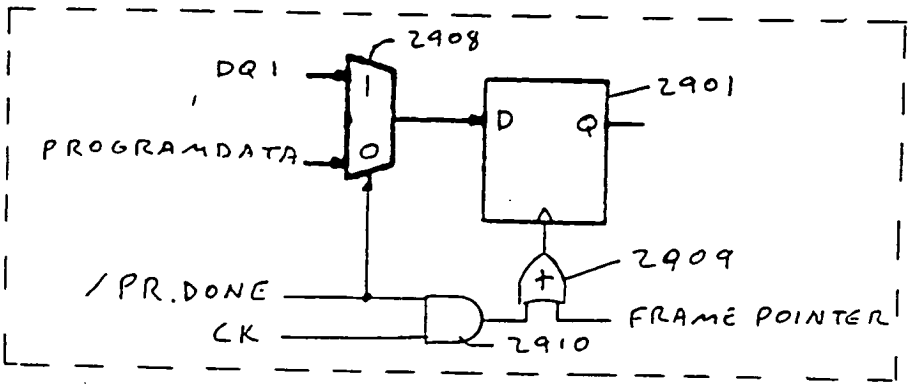


FIG.-29A

MACROCELL 2

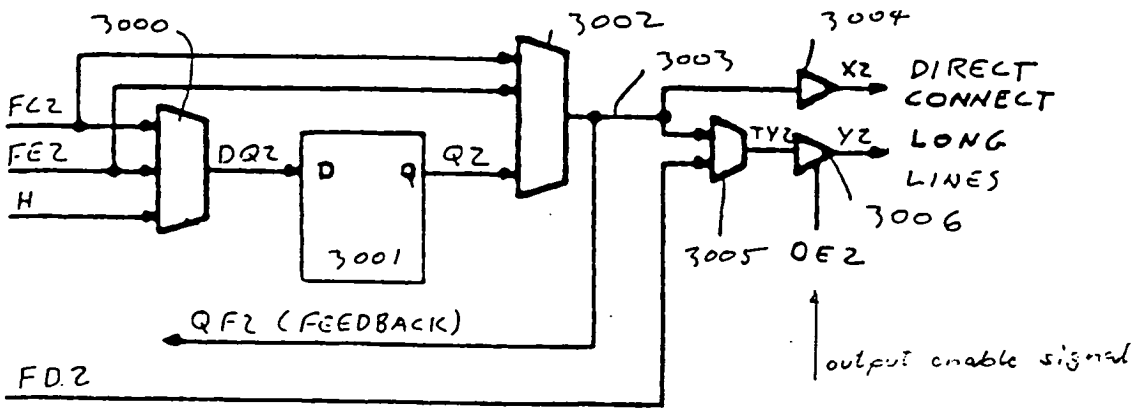


FIG.-30

CLB MACROCELLS

MACROCELL 3

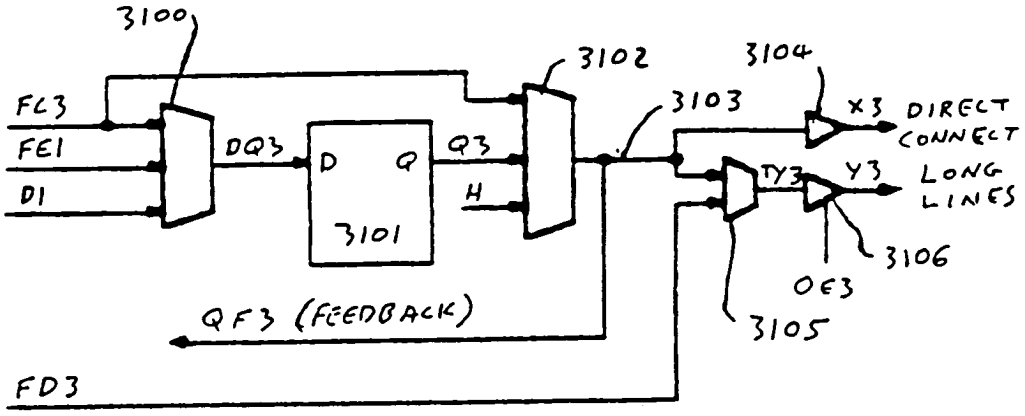


FIG.-31

MACROCELL 4

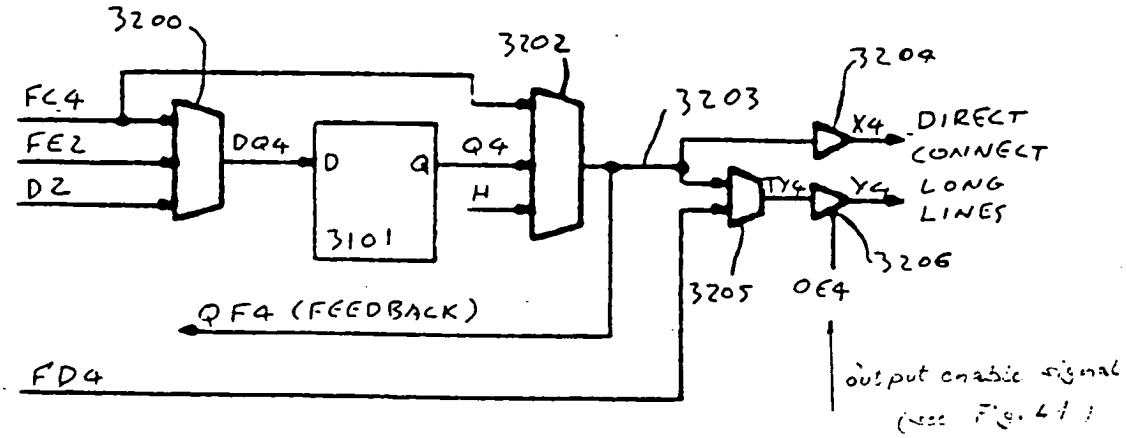


FIG.-32

CLB INPUT MUX'ING

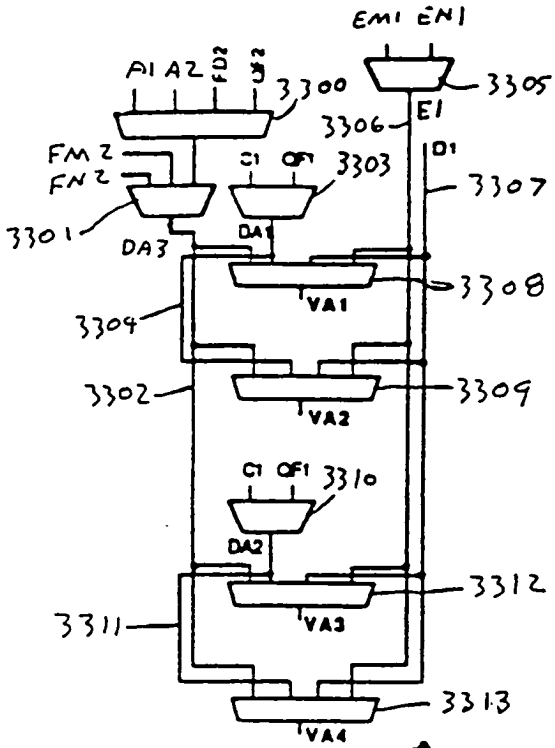


FIG.-33

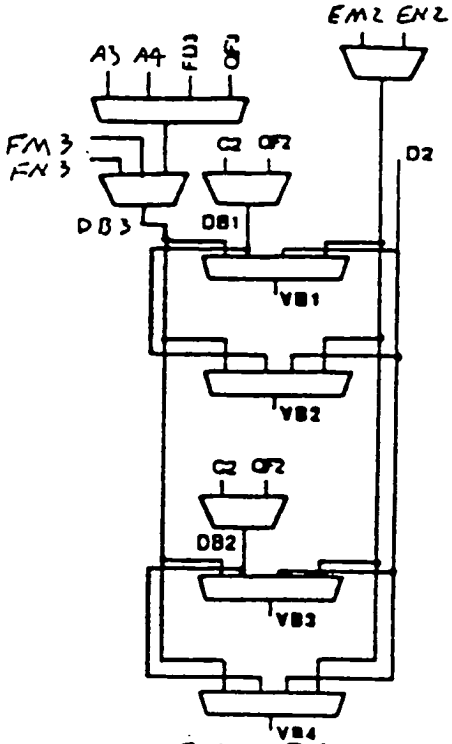


FIG.-34

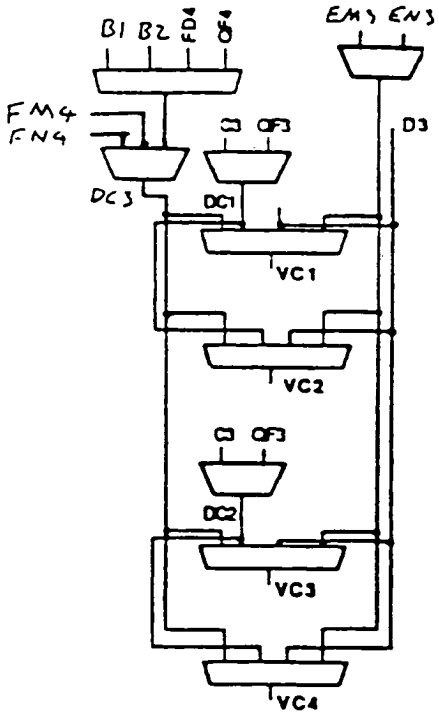


FIG.-35

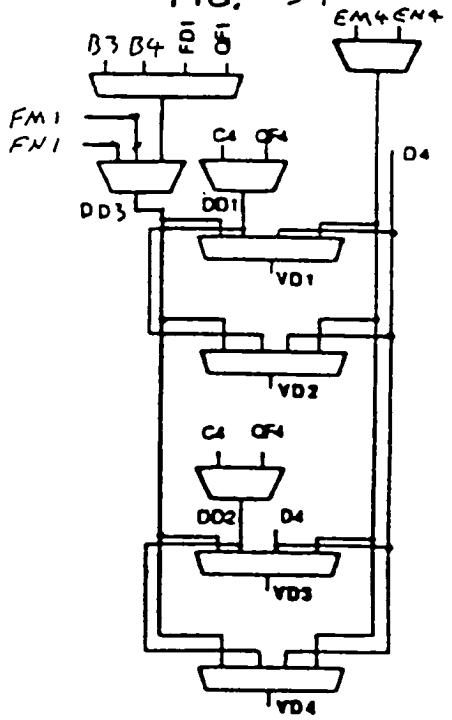


FIG.-36

C L B MUX'ING

3RD LEVEL MUXING

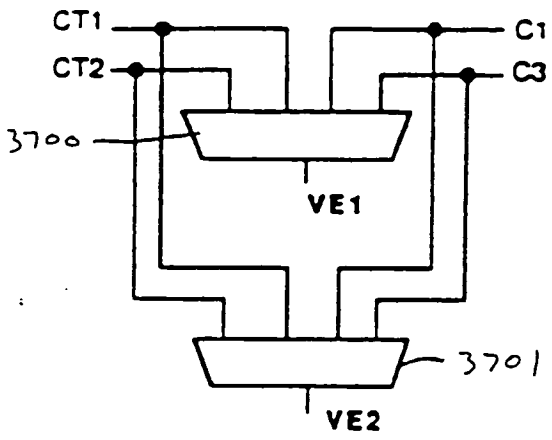


FIG.-37

4TH LEVEL MUXING

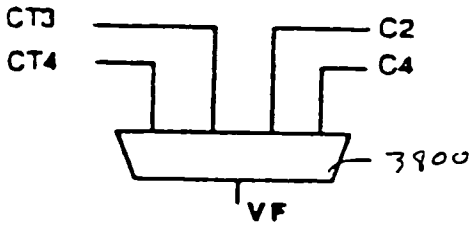


FIG.-38

SPECIAL OUTPUT MUX CONTROL

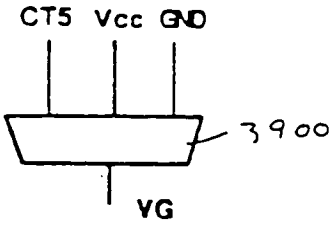


FIG.-39

GENERAL PURPOSE CONTROL LINES

IN CLDS

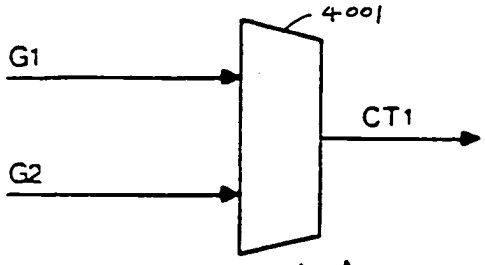


FIG.-40A

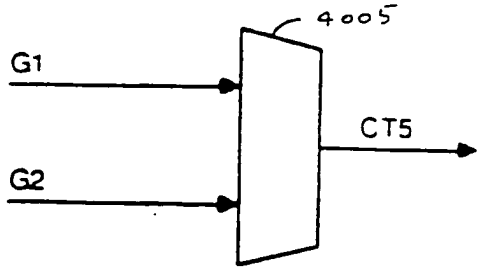


FIG.-40E

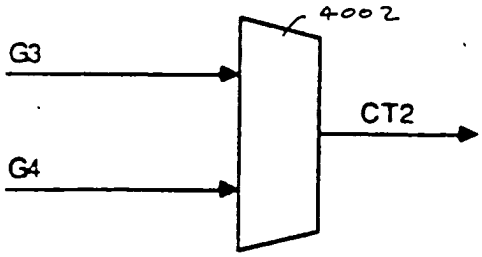


FIG.-40B

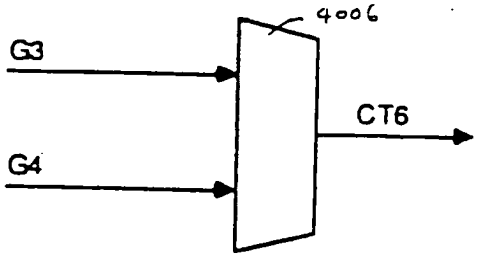


FIG.-40F

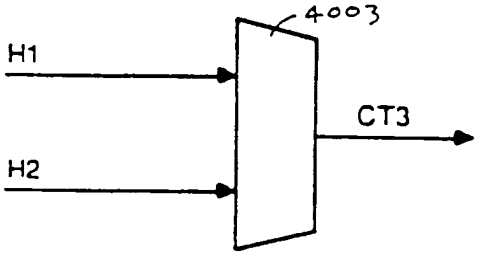


FIG.-40C

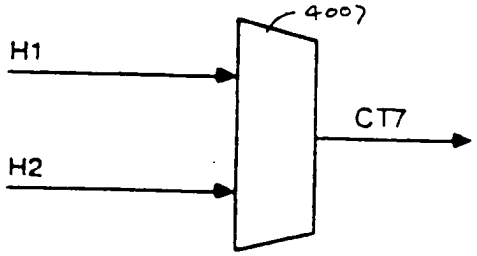


FIG.-40G

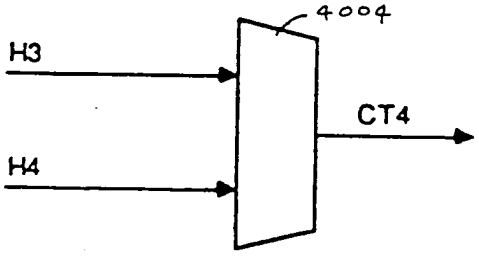


FIG.-40D

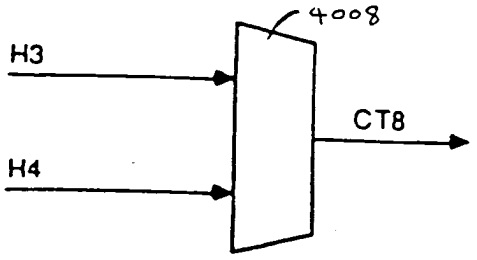


FIG.-40H

CLB MACROCELL CONTROL OPTIONS

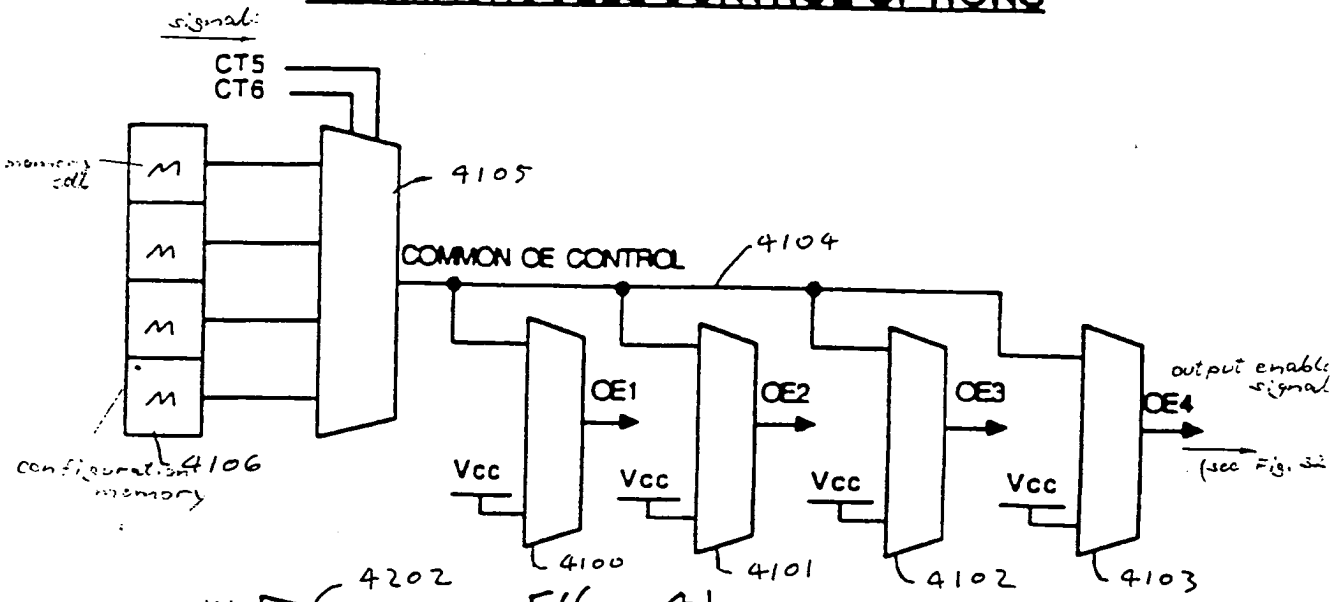


FIG.-41

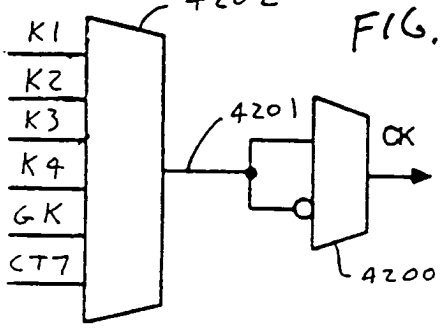


FIG. 42

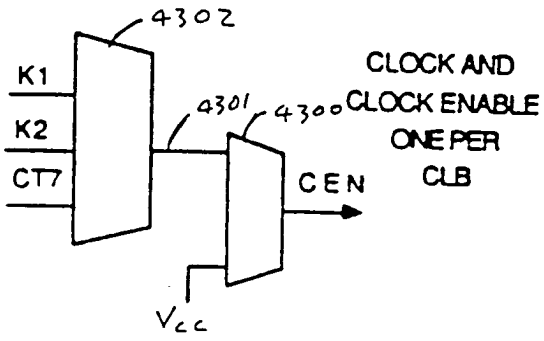


FIG.-43

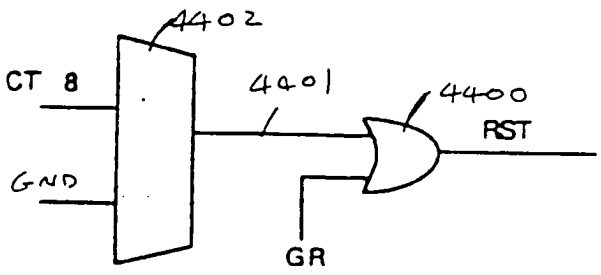


FIG.-44

SIMPLE IO CELL WITH TRISTATE CAPABILITY

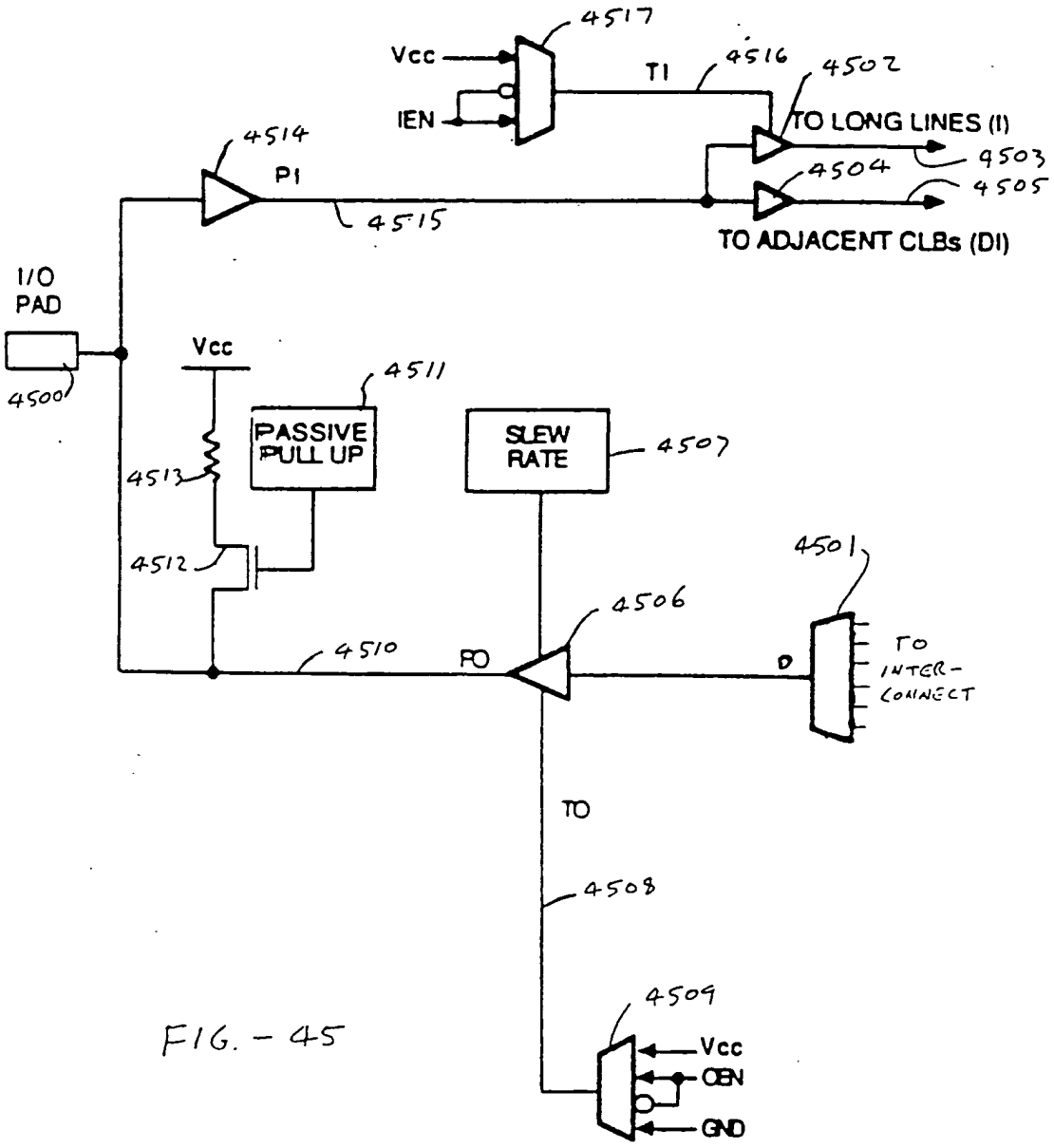
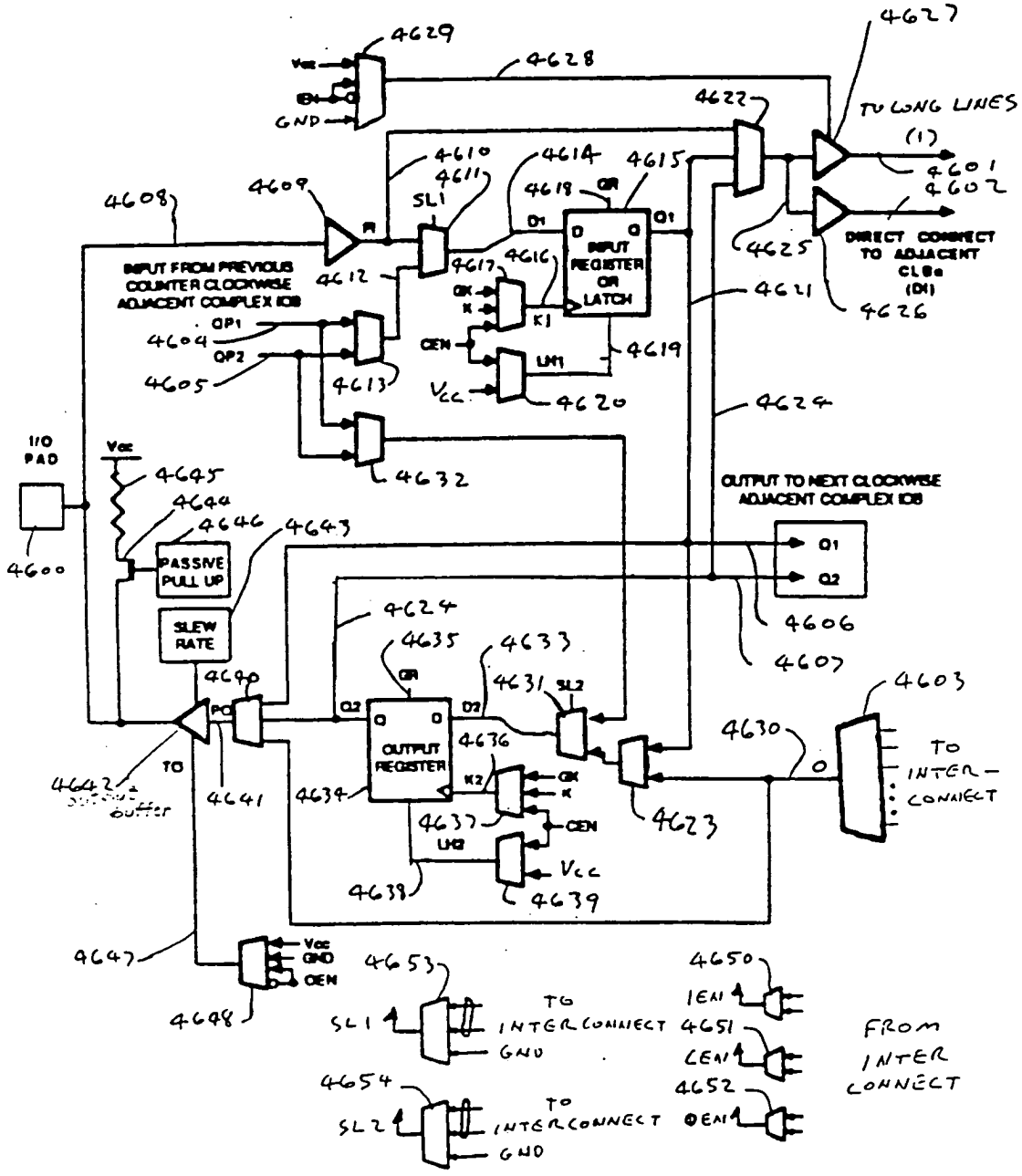


FIG. - 45

I/O WITH TRISTATE CAPABILITY



output enable

FIG.-46

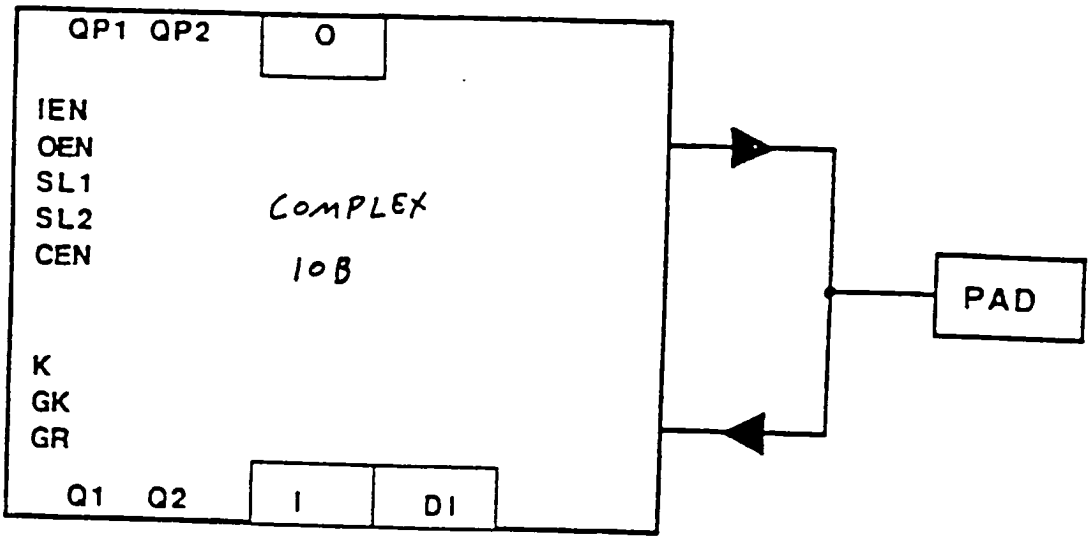

QP1 QP2
O
IEN
OEN
SL1
SL2
CEN
COMPLEX
IOB
K
GK
GR
Q1 Q2
I
DI
PAD

FIG. — 47

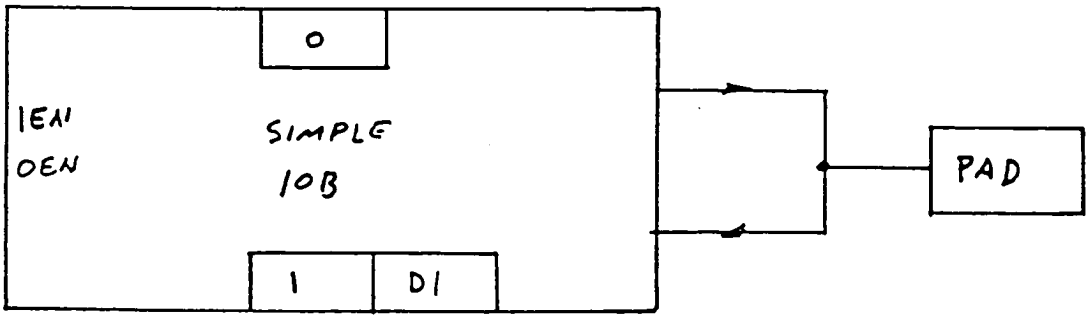

O
IEN
OEN
SIMPLE
IOB
I
DI
PAD

FIG. — 48

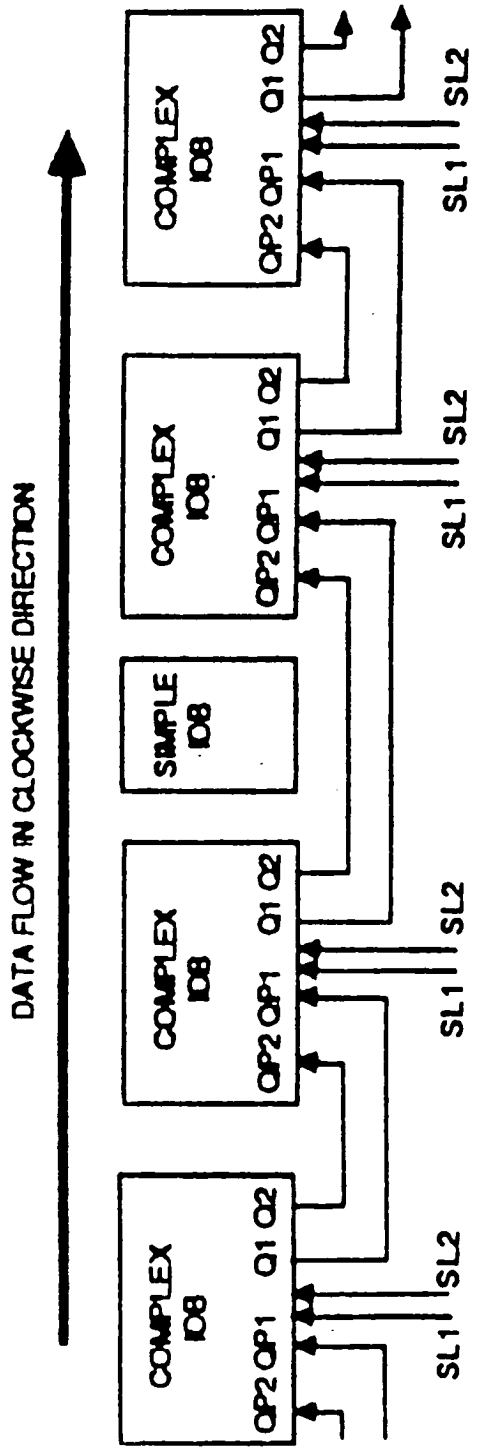

DATA FLOW IN CLOCKWISE DIRECTION
COMPLEX IO8
OP2 OP1 Q1 Q2
SIMPLE IO8
SL1
SL2

FIG. — 49

DIRECT CONNECT FROM NEXT ADJACENT CLBS

(INPUT TO CENTER CLB)

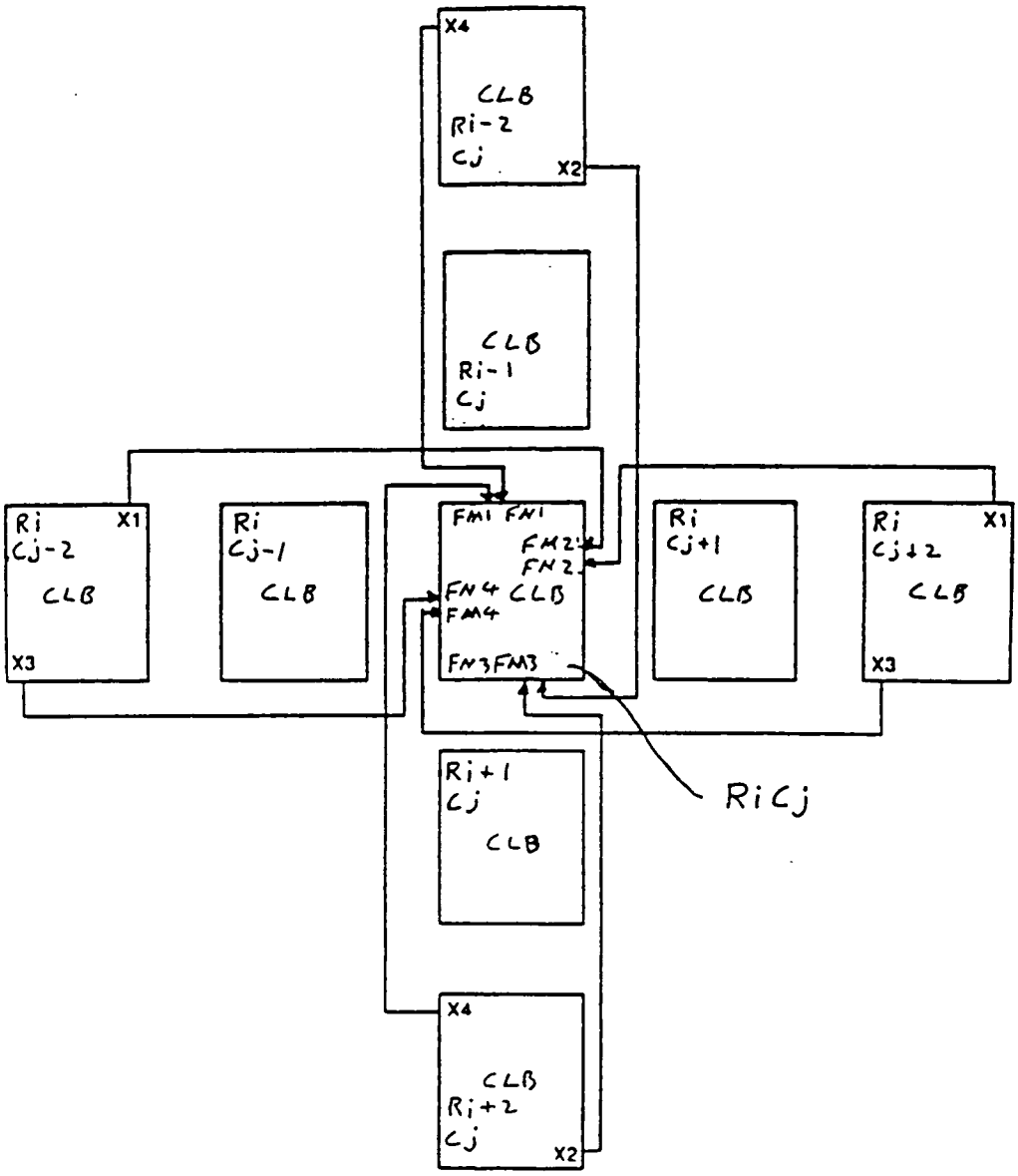


FIG.-50

DIRECT CONNECT FROM ADJACENT CLBS
(INPUT TO CENTER CLB)

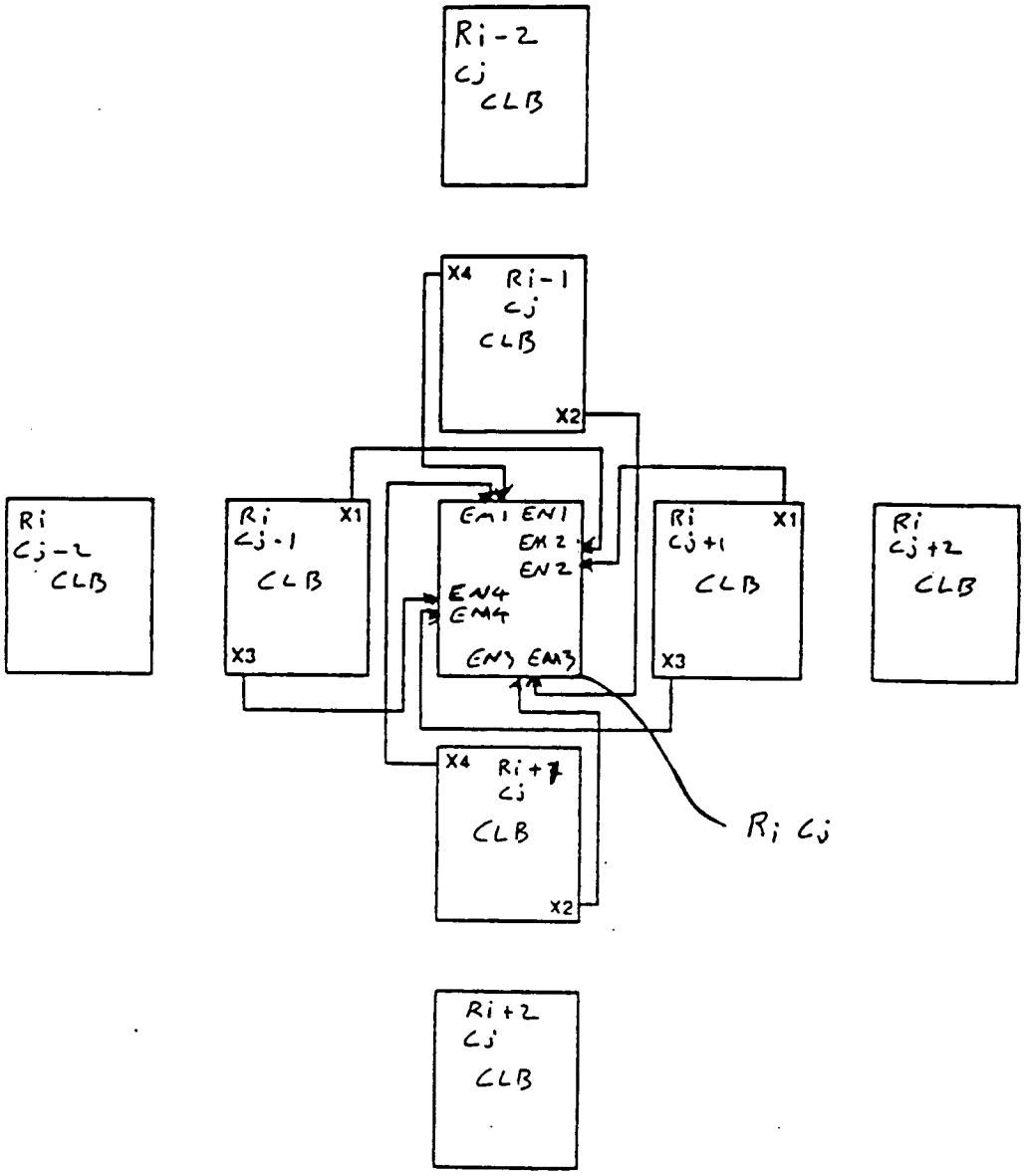


FIG. – 51

DIRECT CONNECT BETWEEN CLBS

(OUTPUT FROM CENTER)

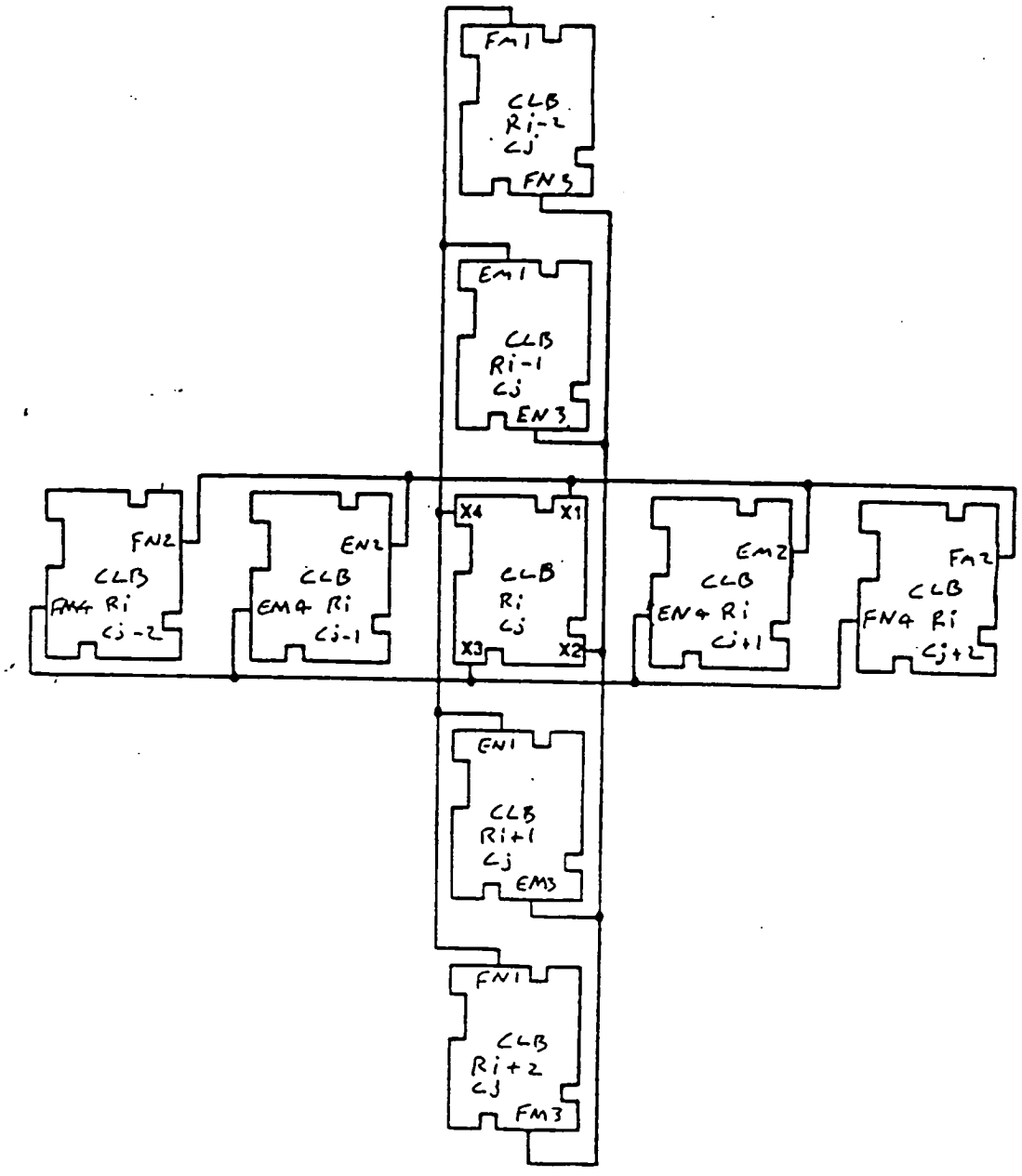


FIG-52

DIRECT CONNECT FROM CLBS TO IOBS

(OUTPUT FROM X1/X2/X3/X4 ON PERIPHERAL CLBS)

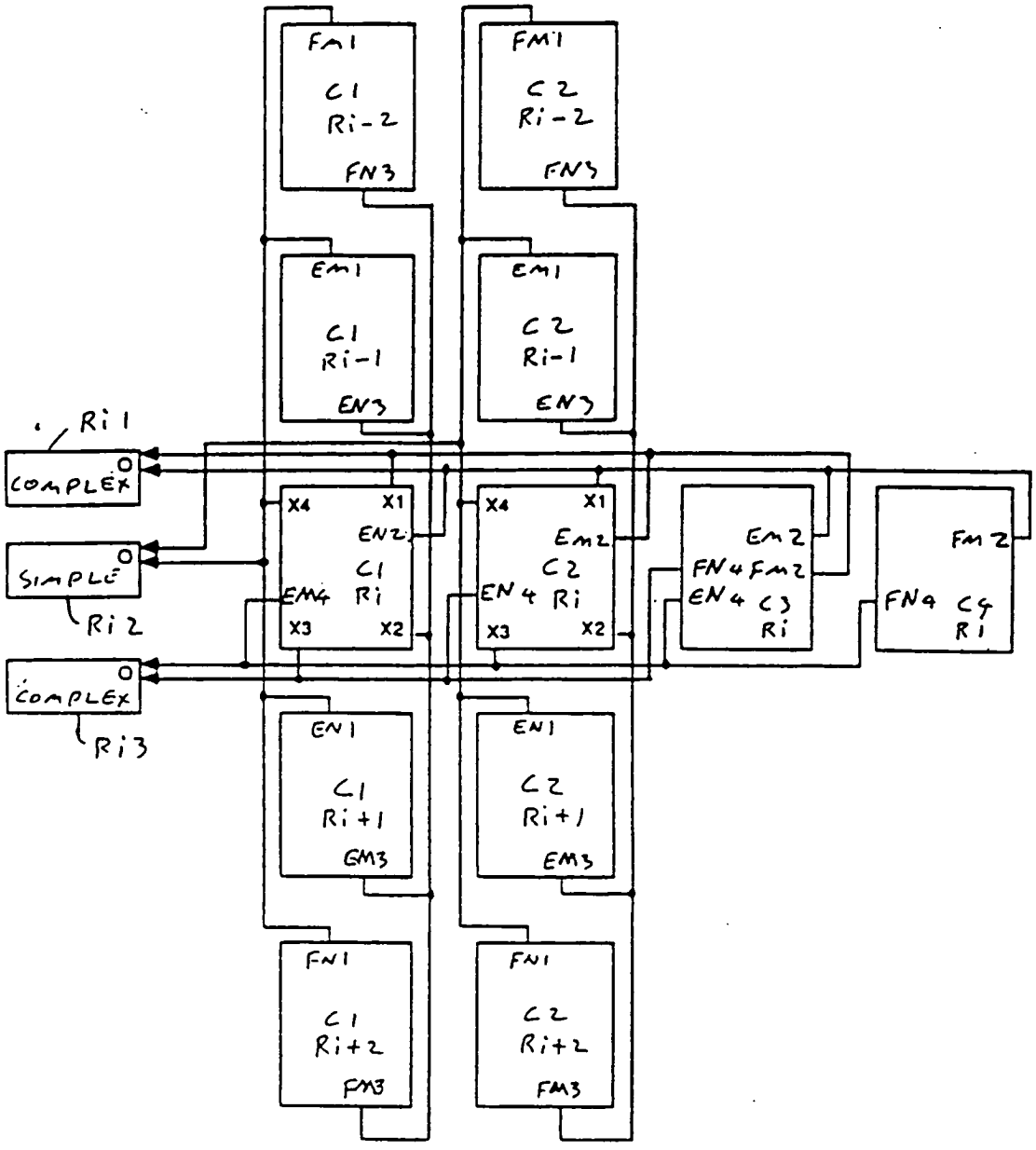


FIG. - 53

DIRECT CONNECT

(INPUT TO EM1→EM4 AND EN1→EN4 ON PERIPHERAL CLBS)

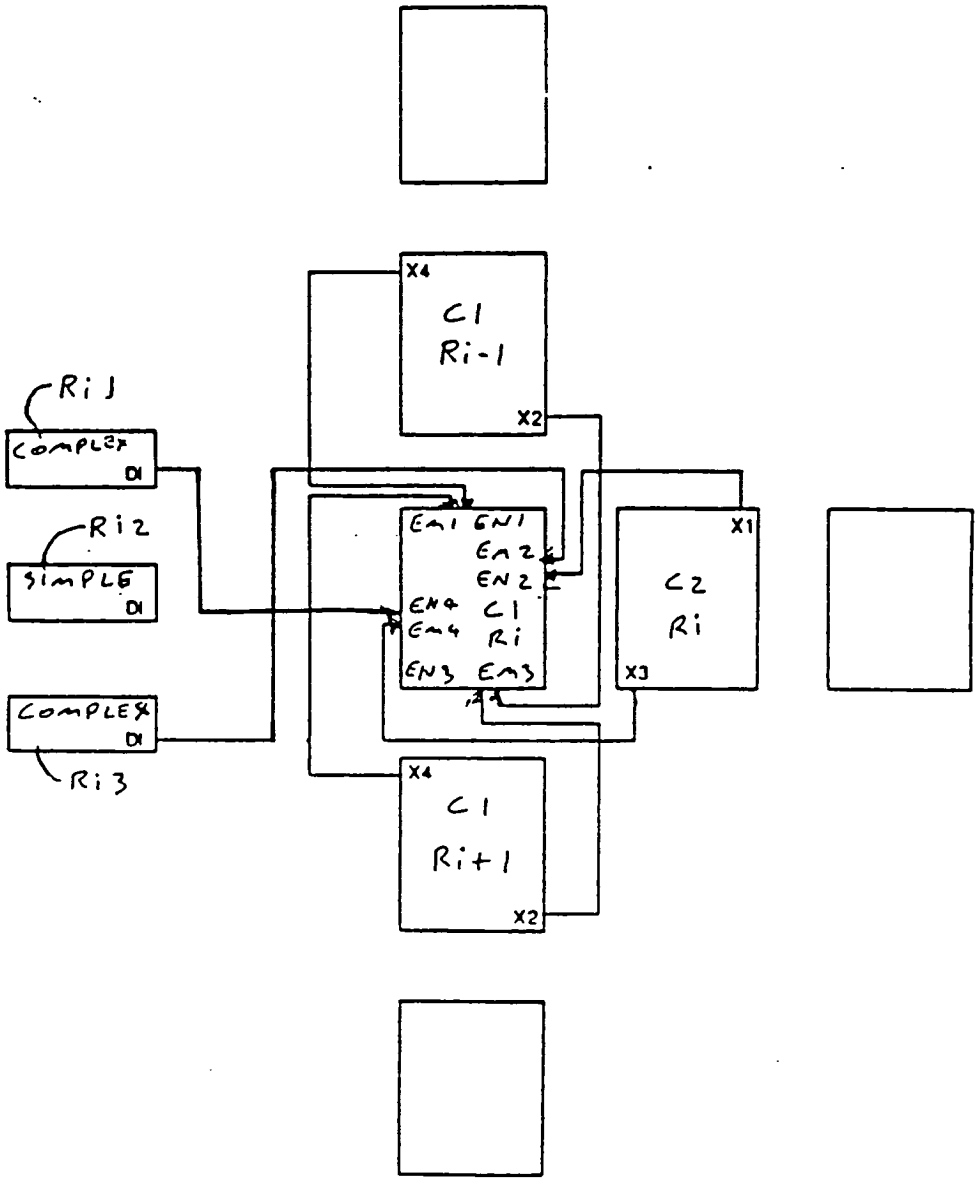


FIG. -54

DIRECT CONNECT

(INPUT TO FM1 – FM4 AND FN1 → FN4 ON PERIPHERAL CLBS)

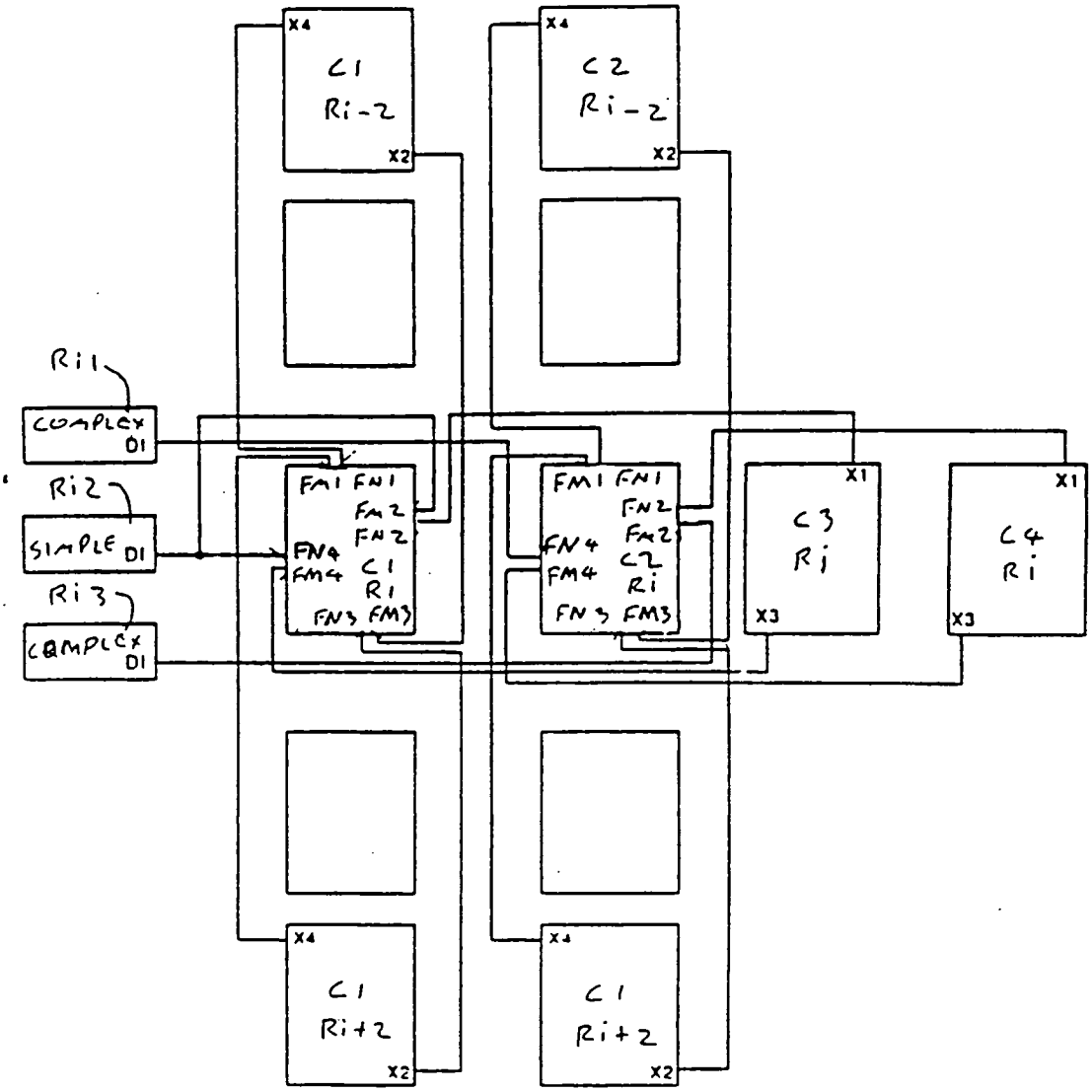


FIG. – 55

CLB PROGRAMMABLE GENERAL INPUTS AND OUTPUTS

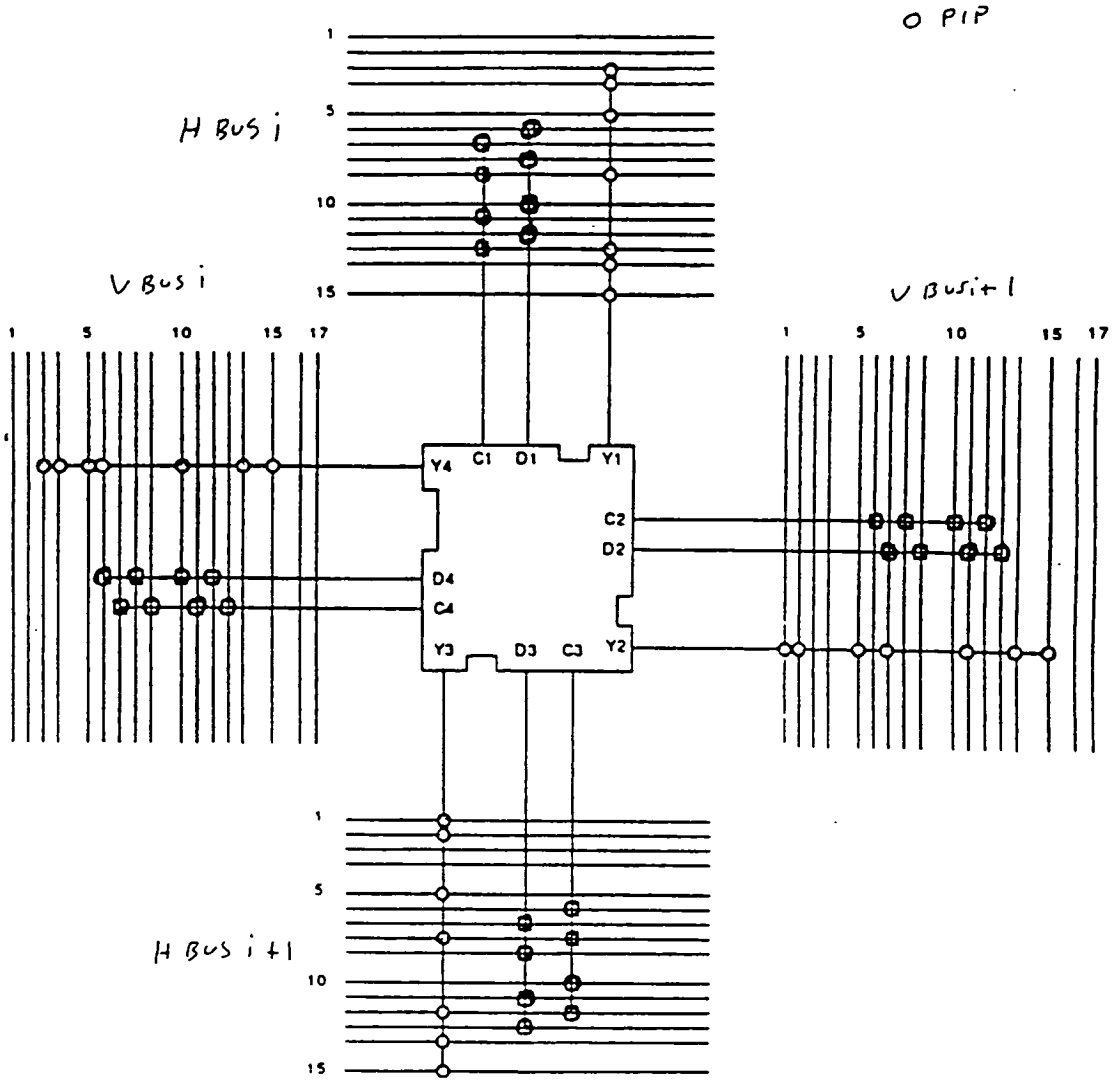


FIG. 56

FIXED INPUTS TO CLB

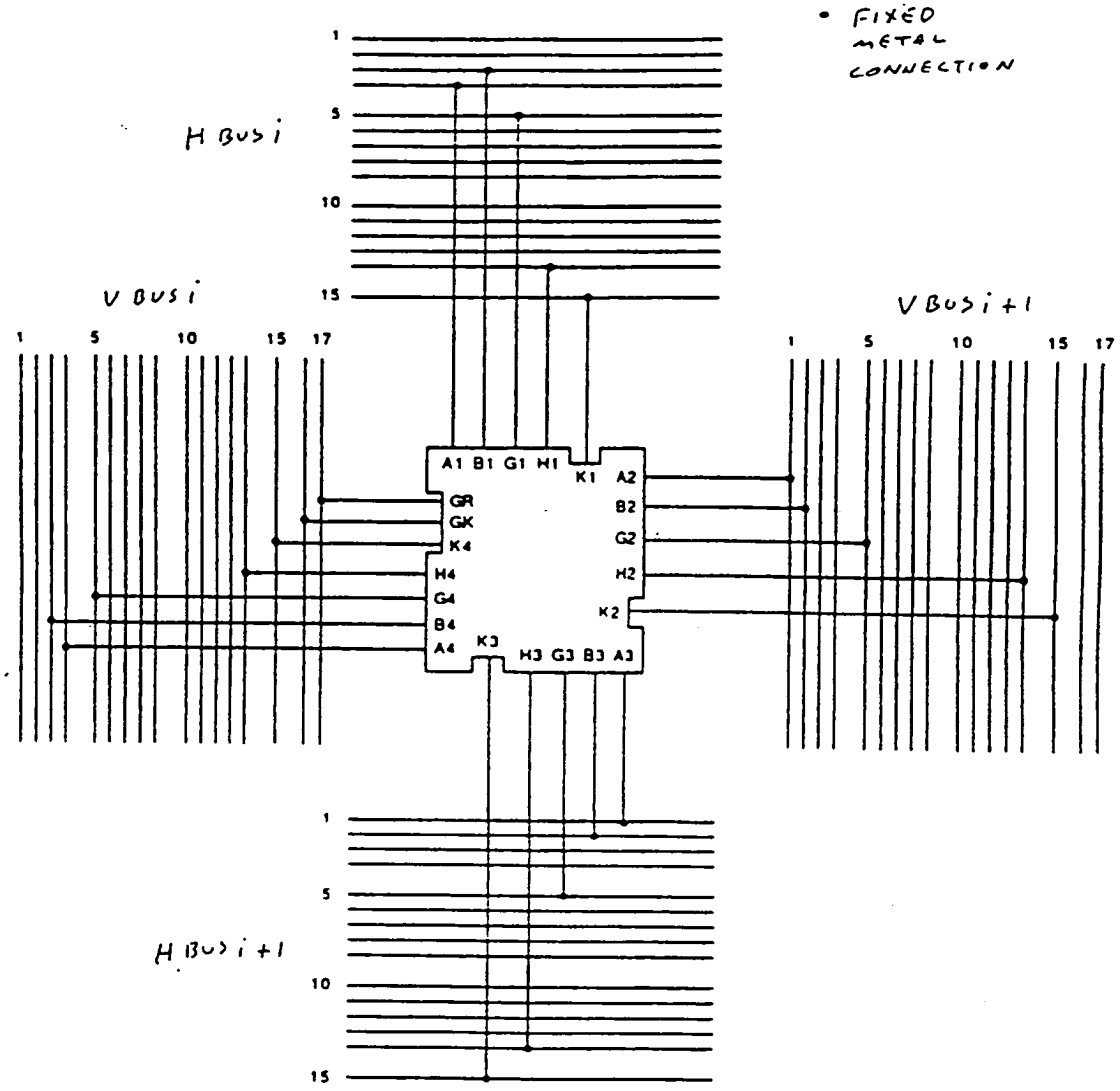


FIG. — 57

CLB TO UNCOMMITED LONG LINES

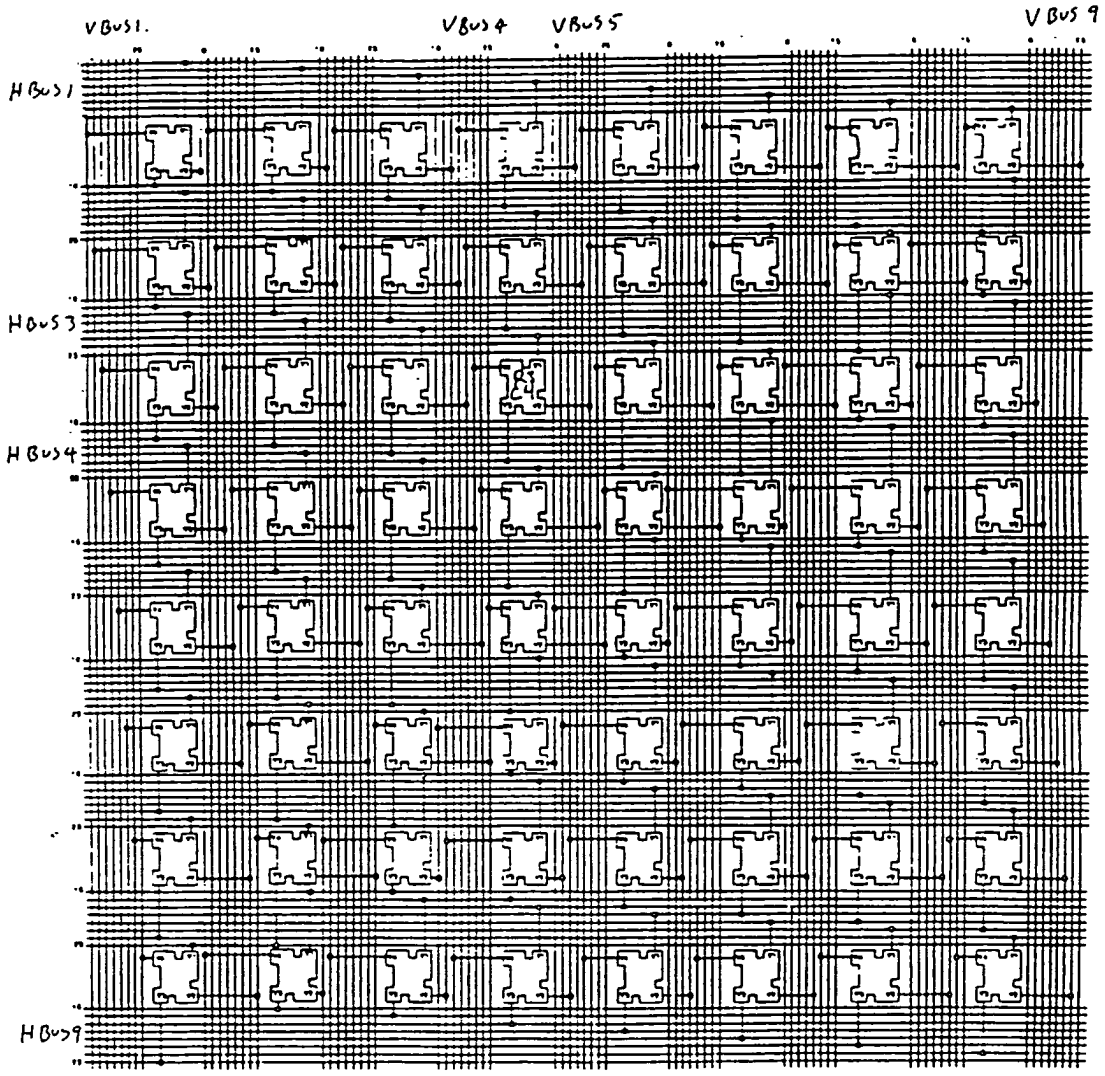


FIG.-58

OUTER LONG LINE DRIVE FROM CLBS

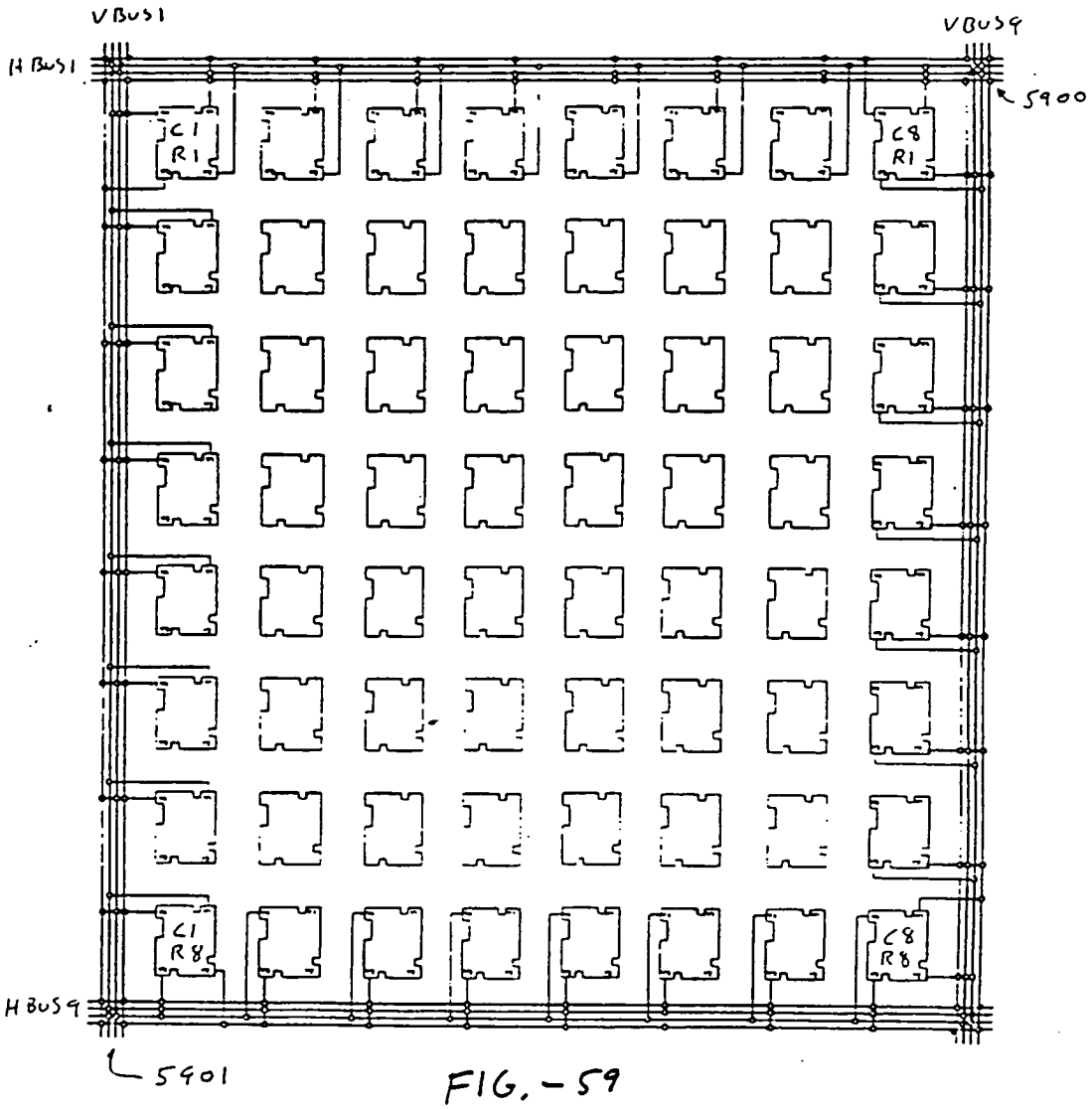


FIG. - 59

LONG LINE REACH BETWEEN IOBS AND CLBS

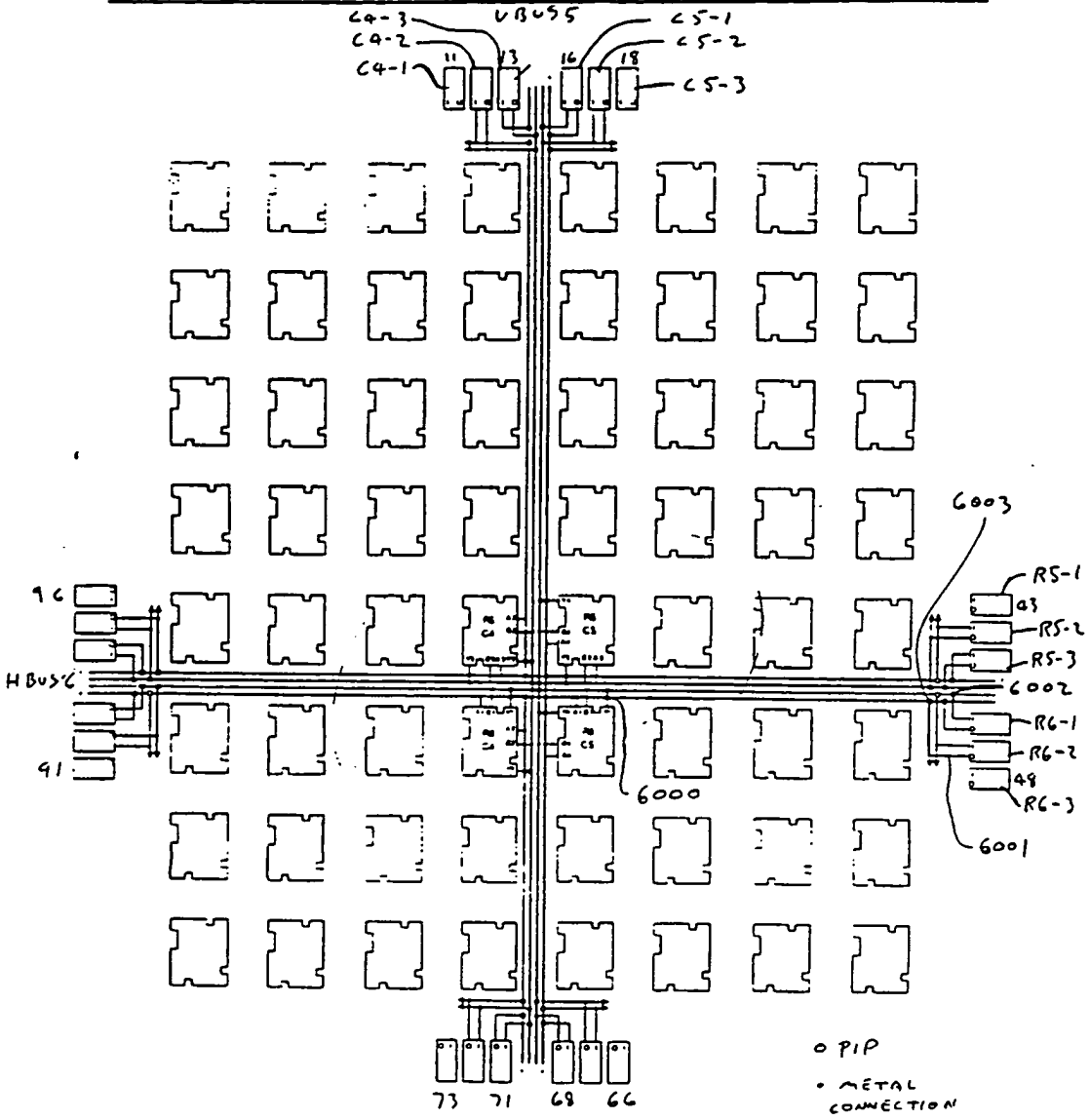


FIG.—60

IOB CONNECTIONS - TOP SIDE TO HORIZONTAL BUS1

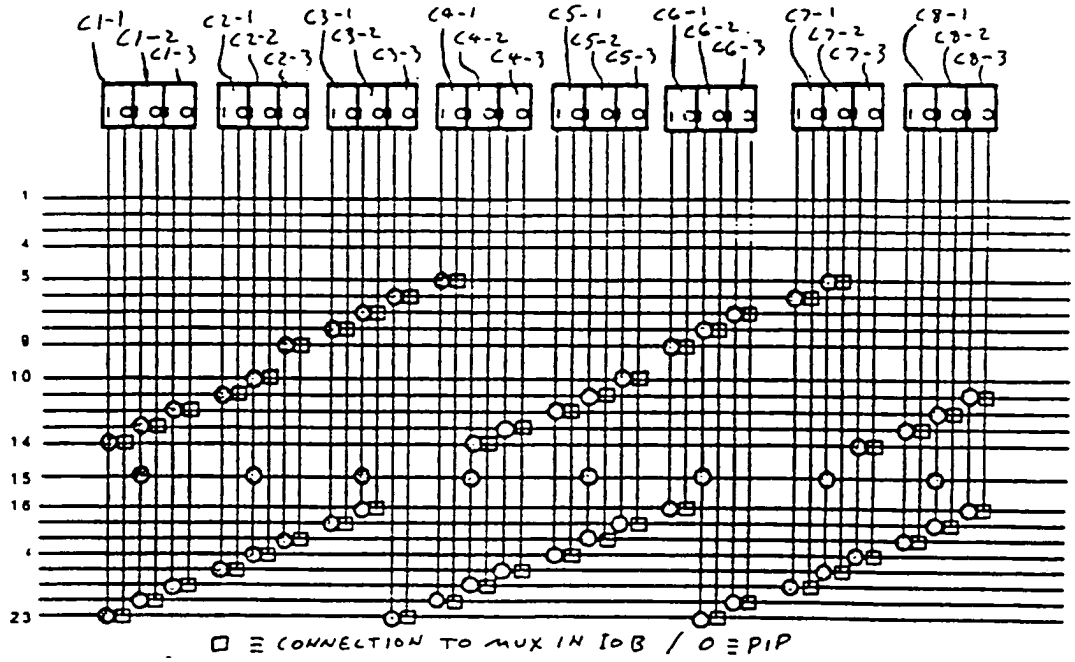


FIG.-61

IOB CONNECTIONS - BOTTOM SIDE TO HORIZONTAL BUS9

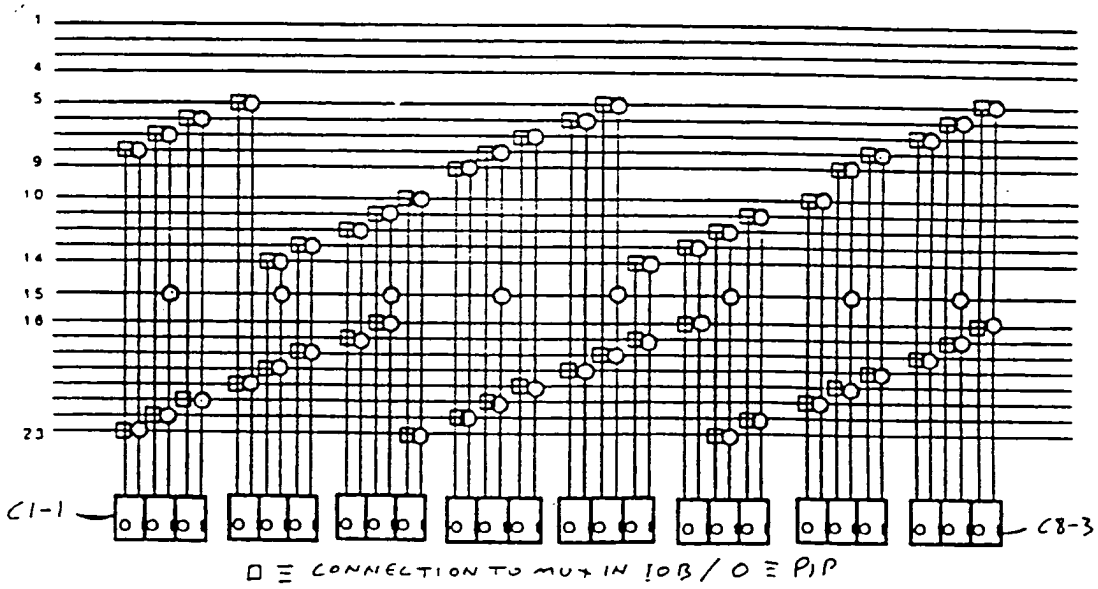


FIG.-62

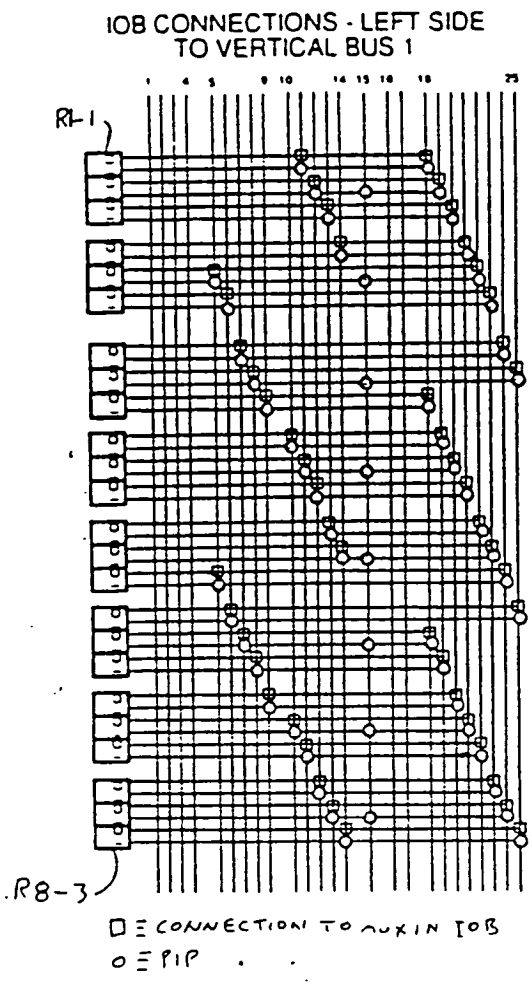

IOB CONNECTIONS - LEFT SIDE
TO VERTICAL BUS 1
R1-1
R8-3
□ = CONNECTION TO MUX IN IOB
○ = PIP

FIG.-63

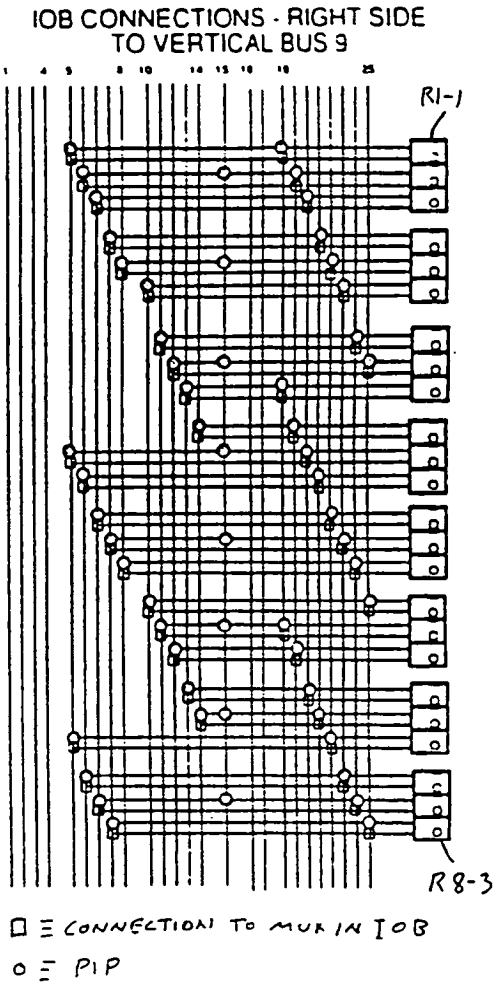

IOB CONNECTIONS - RIGHT SIDE
TO VERTICAL BUS 9
R1-1
R8-3
□ = CONNECTION TO MUX IN IOB
○ = PIP

FIG.-64

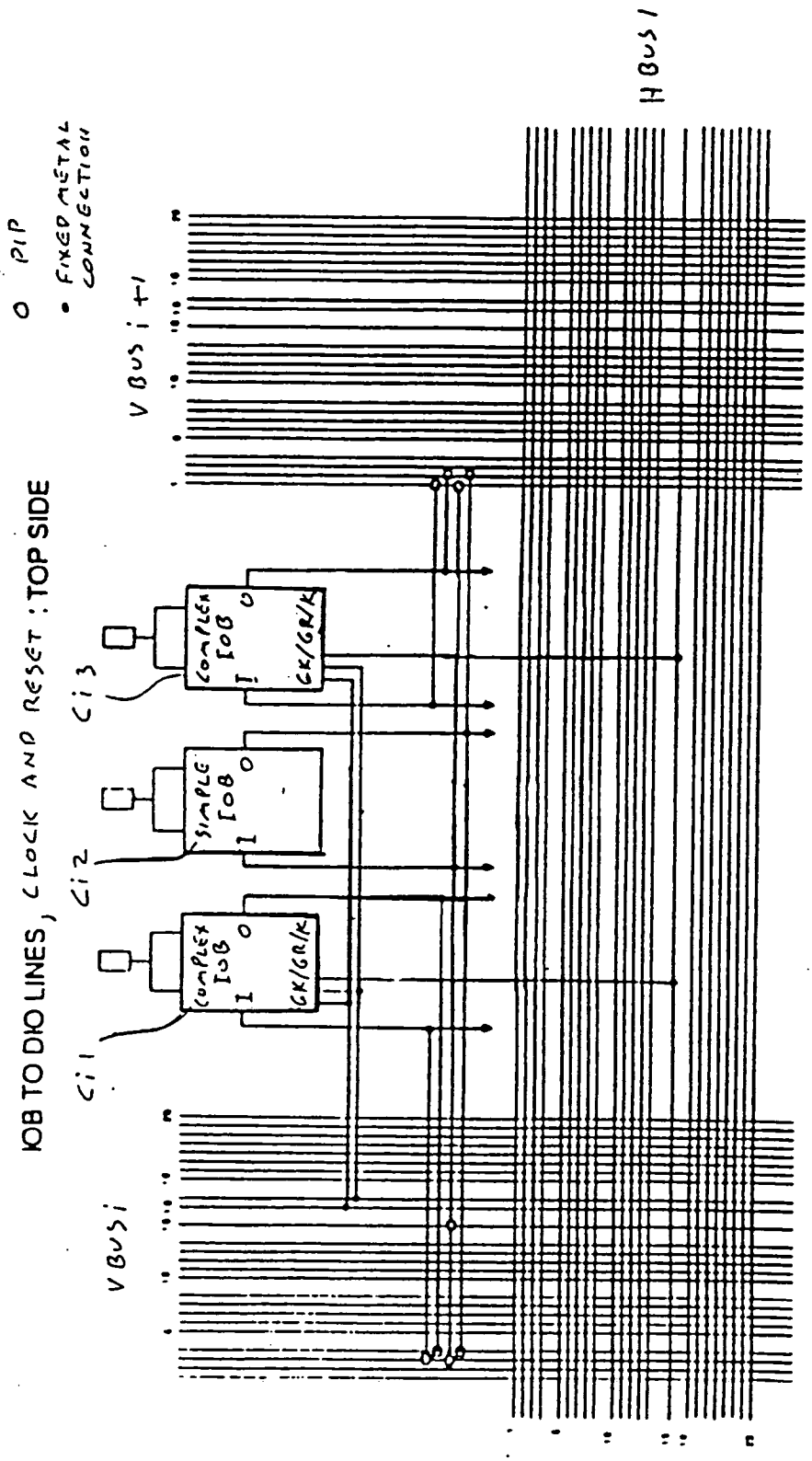

IOB TO DIO LINES, CLOCK AND RESET : TOP SIDE
O PIP
• FIXED METAL CONNECTION
V BUS i
V BUS i+1
H BUS j
Ci1
Ci2
Ci3
COMPLEX IOB
SIMPLE IOB
GK/GR/K

FIG.-65

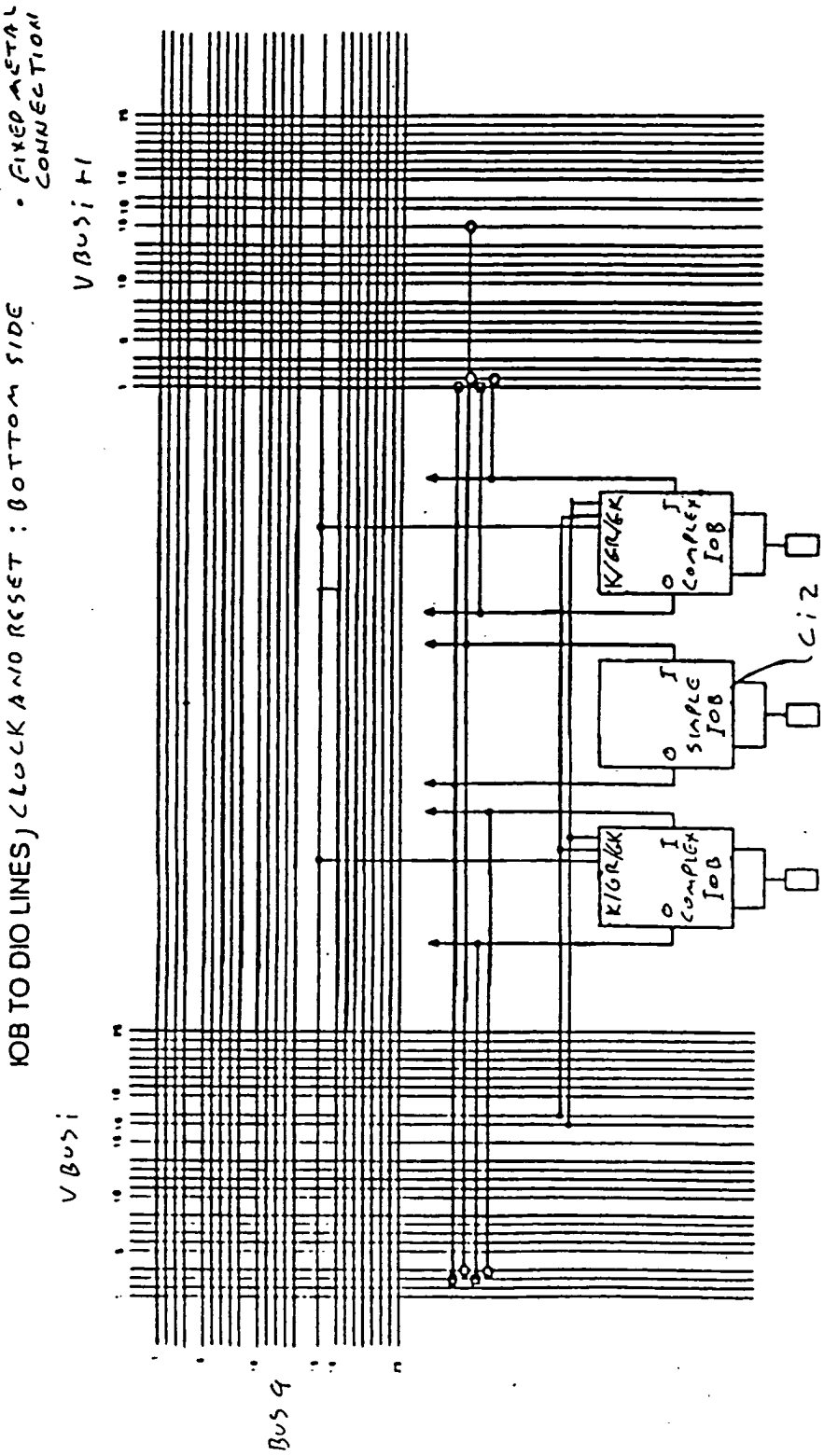

IOB TO DIO LINES, CLOCK AND RESET : BOTTOM SIDE
o PIP
• FIXED METAL CONNECTION
V BUS i+1
V BUS i
BUS q
K/GR/GK
COMPLEX IOB
SIMPLE IOB
K/GR/GK
COMPLEX IOB
I
O
I
O
I
O
Ci2

FIG. - 66

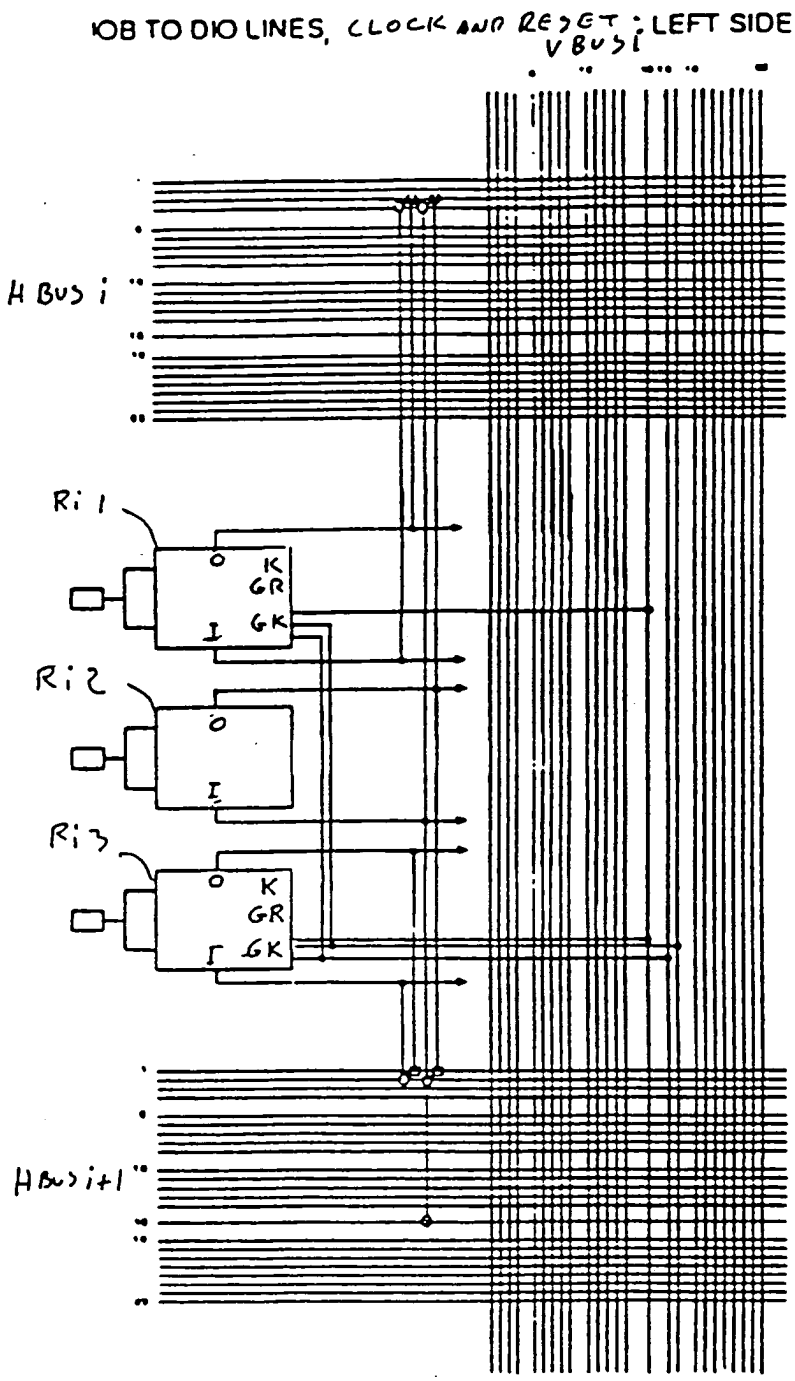

IOB TO DIO LINES, CLOCK AND REGET ; LEFT SIDE
V Bus j
H Bus i
Ri 1
K
GR
GK
I
Ri 2
Ri 3
H Bus i+1
o PIP
• FIXED METAL CONNECTION

FIG.-67

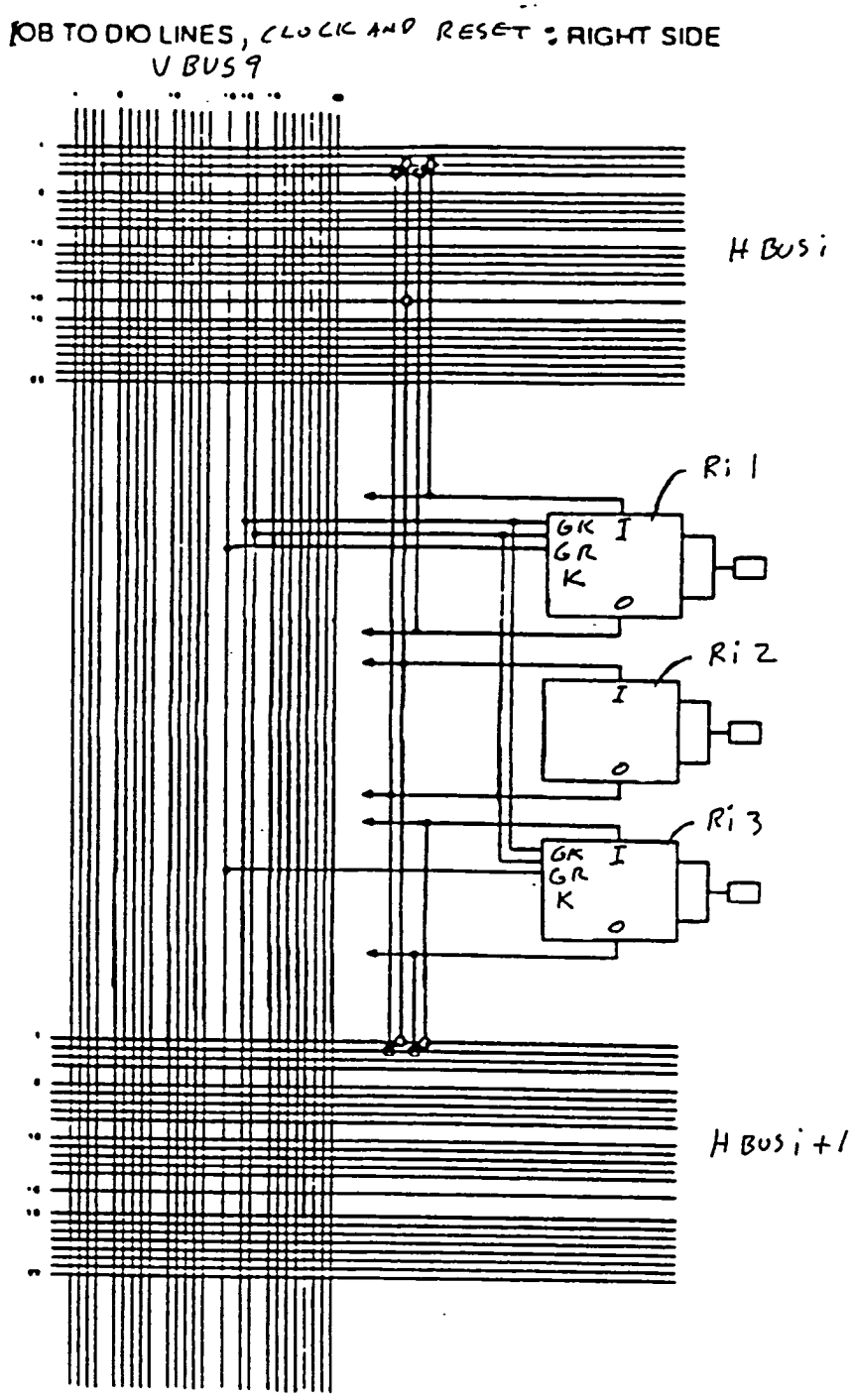

JOB TO DIO LINES, CLOCK AND RESET : RIGHT SIDE
V BUS 9
H BUS i
Ri 1
GK
GR
K
I
O
Ri 2
I
O
Ri 3
GK
GR
K
I
O
H BUS i+1

FIG.-68

IOB CONTROL INPUTS

IOBs AT TOP AND LEFT

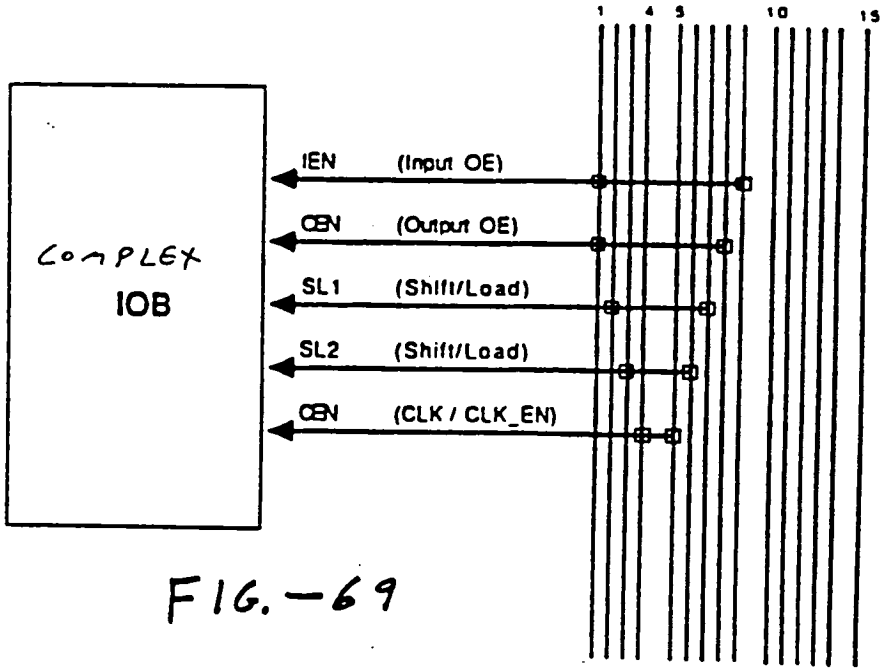


FIG.-69

IOBs AT RIGHT AND BOTTOM

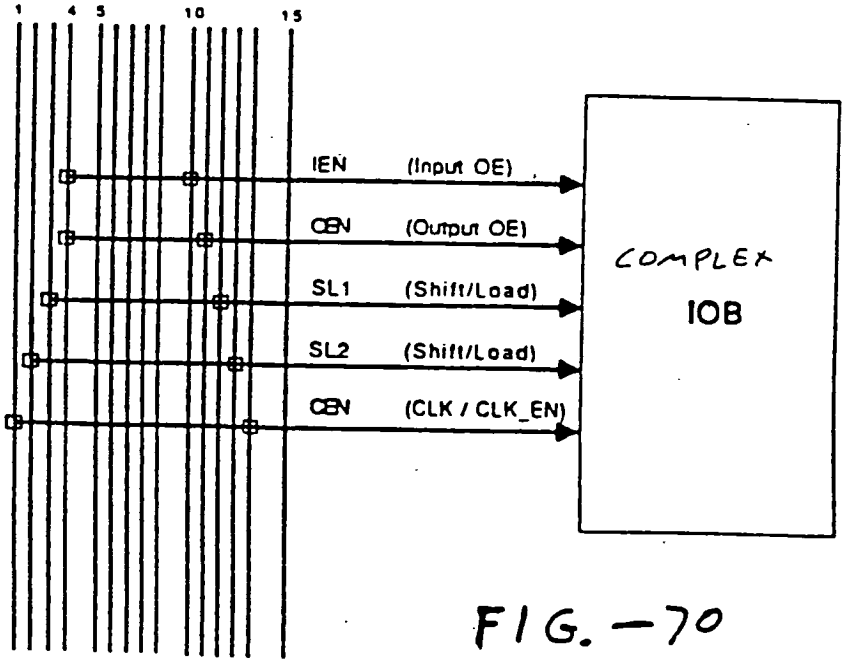


FIG.-70